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Configuring Current Sharing on the ZL6105 and ZL8101

Introduction

This application note describes the features and setup procedure for the ZL6105 and ZL8101 digital DC controllers configured in current sharing groups. These products employ an inter-device communication Bus called the Digital-DC bus (DDC Bus). The DDC Bus enables Intersil Zilker Labs IC's to exchange critical real-time telemetry to any device connected to the Bus. The DDC Bus enables advanced power management, fault management, sequencing, and many other features.

Overview

A current sharing group is comprised of 2 or more parallel converters operating at the same frequency, but interleaved in such a way to multiply the input and output ripple frequency by the number of paralleled phases. Paralleling converters in this manner has the added benefits of reducing the input filter stress, distributing the converter thermal load, reducing volume and weight and many other advantages. Figure 1 is a typical example of a 2-phase current sharing group. Multiple current sharing groups and power rails can communicate and connect to the same DDC Bus.

DDC Bus

Zilker Labs (Digital-DC) products utilize a unique dedicated serial bus (DDC bus) to synchronize and communicate real-time events to other Zilker Labs devices connected to the bus. A 5-bit address is assigned to each DDC Bus controller based on the 5 LSB's of its SMBus address and comprises the Rail DDC ID#. This Rail DDC ID# is used to specify which controllers on the same DDC Bus listen and respond to Fault Spreading and Sequencing.

The Rail DDC ID# is automatically assigned as the IShare Rail ID in the ISHARE_CONFIG command. However, the IShare Rail ID number must be common to each controller in the current sharing group and not used to define any other output rail. Table 1 below serves as an example for the current sharing group in Figure 1. In this example the IShare Rail ID has been arbitrarily assigned a value of 5.

TABLE 1. CONFIGURING ISHARE RAIL ID#

PMBUS ADDRESS	BINARY	5 LSBs	RAIL DDC ID	ISHARE RAIL ID
0x21	00100001	00001	1	5
0x22	00100010	00010	2	

Table 2 illustrates the complete structure of the ISHARE_CONFIG field.

A maximum of 7 devices or phases is allowed in a sharing group. Please ensure that the DDC signal integrity is maintained by adjusting the pull-up resistor value when using a large device count.

TABLE 2. COMPLETE ISHARE_CONFIG FIELD

ISHARE_CONFIG			
BITS	**PURPOSE**	**VALUE**	**DESCRIPTION**
15:8	IShare Rail ID	0 to 31 (0x00 to 0x1F	Sets the current share rail's DDC ID for each controller within a current share rail. Each controller in the sharing group must have the same IShare Rail ID
7:5	Number of Devices	0 to 7	Number of devices in current share rail -1
4:2	Device Position	0 to 7	Position of device within current share rail
1	Reserved	0	Device is not a member of a current share rail
0	Current Share Control	0	Device is not a member of a current share rail
		1	Device is a member of a current share rail

During DDC events, all devices will receive transmissions, however, only those devices configured to respond will do so. DDC devices can also transmit events if the configuration requires inter device communication. Some examples include fault spreading, sequencing, phase add/drop, broadcast margin, broadcast enable, and auto compensation.

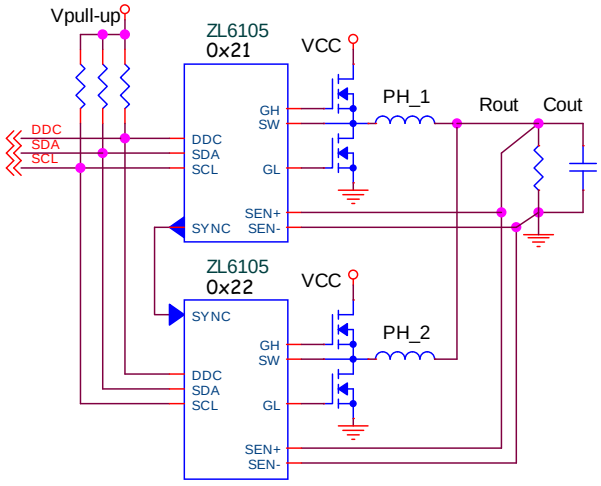

FIGURE 1. TYPICAL CURRENT SHARING APPLICATION

Active Droop Current Sharing

Zilker Labs current sharing devices use a patented form of digitally controlled active droop, resulting in the highest degree of phase current balancing. The specific droop is configured based on the application and is set to the same value for each group member.

The droop function is implemented in both hardware (fast and local) and firmware (slow over DDC Bus). During turn-on/off a combination of droop and a unique ramping algorithm results in near perfect current sharing. The specific value of droop typically ranges between 0.15mΩ and 1mΩ. Each controller in the sharing group is assigned the same droop value. The droop value represents the output loadline. If phases are added or dropped the rail loadline remains constant. Droop is configured with the VOUT_DROOP command, units are in mV's.

Reference Device

The controller with the lowest SMBus address in the current sharing group is designated as the Reference Device. The Reference Device continuously broadcasts its inductor current over the DDC bus, while each Member device receives the transmission and trims its output voltage up or down until all group members supply the same current to the load. The process of broadcasting the Reference's load current and trimming each Member's output voltage to achieve current balance continues unless a fault occurs or the Reference Phase is dropped.

Current Sharing Algorithm

Figure 2 is an example of a current sharing application whose loadlines were all configured to 1mΩ. Due to differences in layout and component variances the actual member loadlines contain slope differences; they are exaggerated in this example.

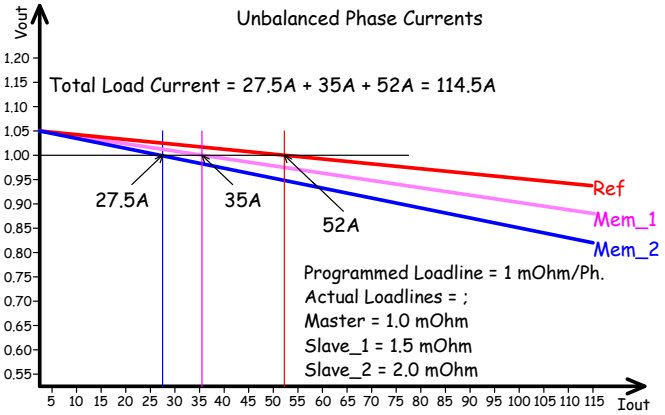

FIGURE 2. UNBALANCED PHASE CURRENTS DUE TO SLOPE ERROR

The imbalance results in each phase contributing an unequal portion of the load current. Each controller will respond to the imbalance with its local hardware droop function and the output voltage will trim down proportionally to constrain the phase current.

After the rail has reached the configured target voltage the DDC Bus will begin to dynamically equalize the phase currents. The Reference Phase controller with the lowest PMBus address periodically broadcasts its current. Each Member Phase(s) reference voltage is trimmed up or down until all devices in the group carry an equal portion of the load current. The current sharing algorithm uses the PMBus Trim command so the Trim command must not be configured by the designer when using current sharing. This effect is shown in Figure 3. Notice in this case the Reference-Phase initially sourced the majority of the load current. Each Member Controller's reference voltage was trimmed in the positive direction until all phase's are sourcing equal current to the load.

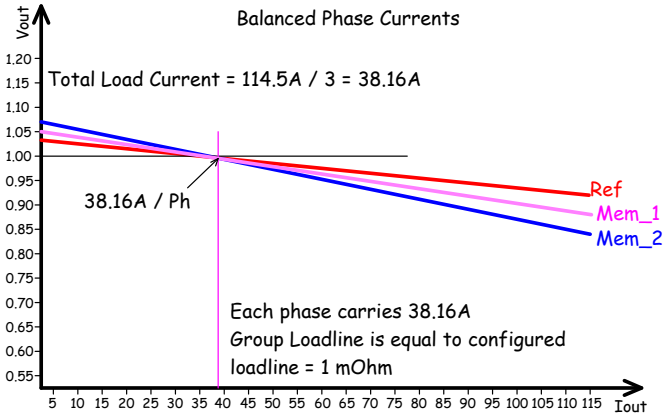

FIGURE 3. MEMBER(S) REFERENCE VOLTAGE IS TRIMMED UNTIL ALL DEVICE CURRENTS EQUALIZE

The Current sharing equilibrium is shown in Figure 4 with a singular loadline being plotted that represents the actual static V-I characteristic for the sharing group. Since each group member in this example is configured to 1mΩ, the slope of the sharing group is equal to 1mΩ.

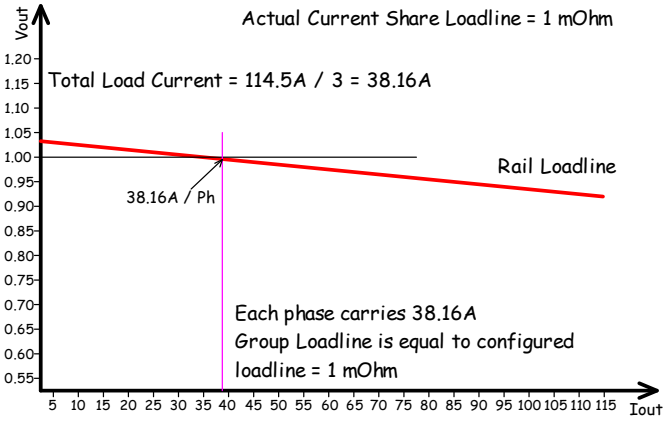

FIGURE 4. CURRENT SHARING PHASE BALANCE IS ACHIEVED

Phase Add/Drop

When Zilker Labs Digital-DC power conversion devices are configured in a current sharing group, individual group members are capable of (dynamically) dropping and adding back to the group. Group members are typically dropped or added to improve efficiency or to process a fault.

Group members can be added or dropped on the fly by using a separate power management host controller invoking the Phase Control command, actively driving the Phase Enable pin PH_EN, or by using the GUI. Adding and dropping phases may cause a slight output voltage perturbation.

If a phase was dropped due to a fault, the standing phase(s) continue to operate. They will autonomously redistribute their phase relationship and maintain the configured load line. This family of controllers don't provide a protocol to fault the entire sharing group. Each controller must detect the fault and then respond as configured.

Dropped Phase/SYNC CLOCK

If the dropped group member was supplying the SYNC clock, it will continue to do so even though it has become inactive. If the device supplying the SYNC clock dropped from the group and is no longer capable of supplying the clock, the remaining members will detect the absence of SYNC and respond according to their fault spreading configuration. If a host or power system manager is monitoring the group, then SALRT will assert, and the PMBus can be read and will respond with the appropriate fault management alarm as described in the PMBus™ Power System Management Protocol Specification – Part II.

If the dropped phase was the group reference, a new reference will be reassigned based on the lowest SMBus address of the remaining operational members. However, if the dropped reference was supplying the SYNC clock it will continue to do so.

The phase position is defined by the angular offset relative to the rising edge of the SYNC clock and will autonomously redistribute based on the number of standing phases.

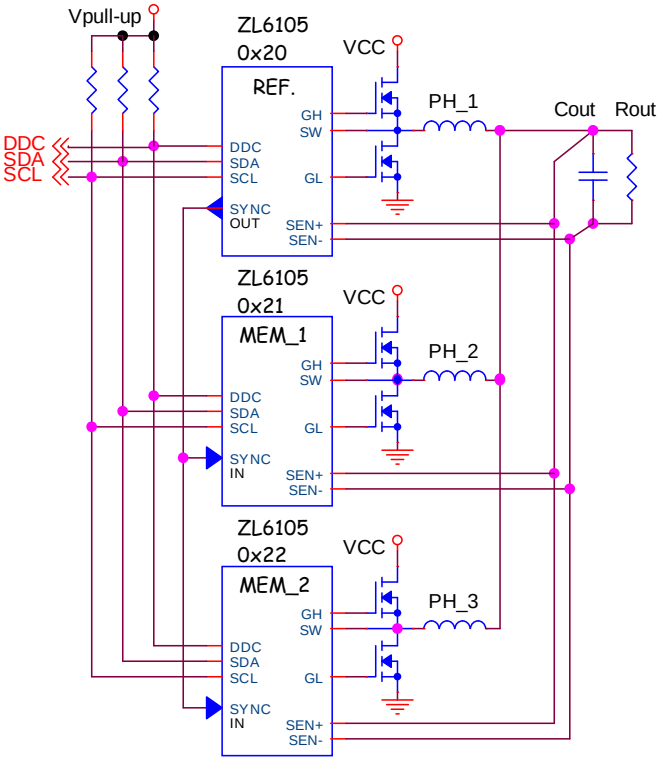

FIGURE 5. 3-PHASE CONVERTER SHOWING REFERENCE, MEMBER, AND POSITION NUMBER

Figure 5 shows an example of a functional 3-phase current sharing group prior to asserting a Phase Control command to drop the Reference Phase (0x20).

Figure 6 illustrates the new 2-phase configuration after the reference phase (0x20) is dropped. Address 0x21 is now the new designated reference. Address 0x20 continues supplying the SYNC clock even though it has been dropped.

The timing diagram is shown in Figure 7. After the reference phase is dropped the remaining two phases are redistributed and the phase displacement changes from 120° to 180°.

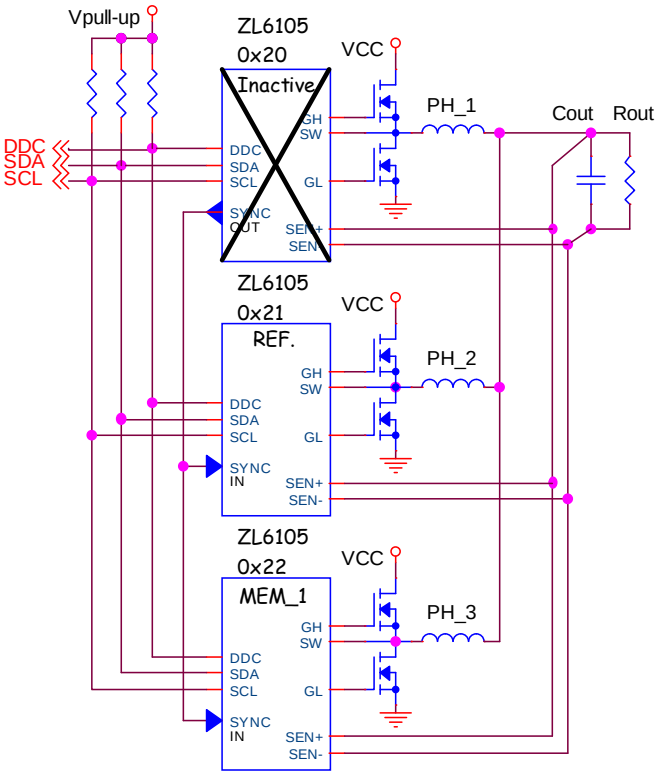

FIGURE 6. 3-PHASE CONVERTER AFTER REFERENCE PHASE IS DROPPED

Phase Add

The phase that was previously dropped may be added back into the group as determined by the power management host or the Phase Control command. When the command is given to add the phase, the event is coordinated with the active member devices over the DDC Bus, and the previously inactive device is seamlessly added back into the group. In this example, position 1 was made active and resumed the role of reference device, see Figure 5. The phase offset of each member was automatically redistributed from 180° to 120° as shown in the top section of Figure 7.

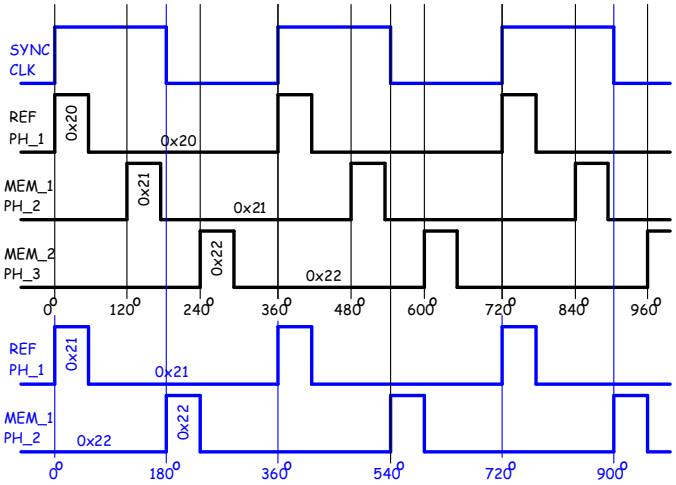

FIGURE 7. 3-PHASE CONVERTER TIMING DIAGRAM BEFORE AND AFTER PHASE_1 (REFERENCE PHASE) IS DROPPED

NLR Threshold Scaling

When multiple devices are configured in a current sharing group, the effective output ripple is divided by the number of active members. When all members of the group are operating, the NLR (Non Linear Response) thresholds can be set to a small value just above the minimum ripple amplitude. When a group member is dropped, the ripple amplitude will increase.

In order to avoid spurious NLR activity, the Digital-DC features automatically adjust the NLR thresholds according to the ratio of *active* group members to *total* members of the group (see Equation 1).

$$Vt\_part = Vt\_all * \frac{Nall}{Nactive} \quad \text{(EQ. 1)}$$

Where:

Vt_part is the NLR inner threshold setting used with some group members deactivated

Vt_all is the NLR inner threshold setting configured for the group with all members operating

Nall is the total number of members in the group

Nactive is the number of members active in the group (that is, the number of members not faulted or intentionally deactivated)

Nall and *Nactive* are determined automatically from the group configuration parameters. No additional programming or configuration is required.

Since the available thresholds are quantized to multiples of 0.5% of the configured output voltage, the next higher available threshold is used if the result of the above formula is fractional. For additional information about NLR, please reference AN2032 “NLR Configuration DDC Products”.

SYNC Clock

To configure a current sharing group, a common SYNC clock must be provided to each group member. This SYNC clock can be provided by any Zilker Labs Digital DC device, or the SYNC can be provided by an external source that satisfies the electrical specifications of the SYNC pin. **Note**: the switching frequency of each ZL Controller must be configured to the same value.

Once the SYNC source has been designated, the SYNC pins of all group members and any other Zilker Labs device requiring synchronization and interleaving must be connected together as shown in Figure 8. Note that any of the devices whose SYNC pins are physically connected together can be configured to output the SYNC clock. The SYNC output can be configured as push-pull or open-drain. All other devices connected to the SYNC source must be configured as SYNC inputs. If the SYNC source becomes disabled while the current sharing rail is enabled, each sharing device will reconfigure to use its internal clock. During the transition small output voltage perturbations might occur. SALRT will assert and the loss of SYNC status register will set. If the output voltage perturbation does not cause a UV fault the current sharing rail will continue to operate. The loss of intra-controller synchronization will cause a small modulated envelope.

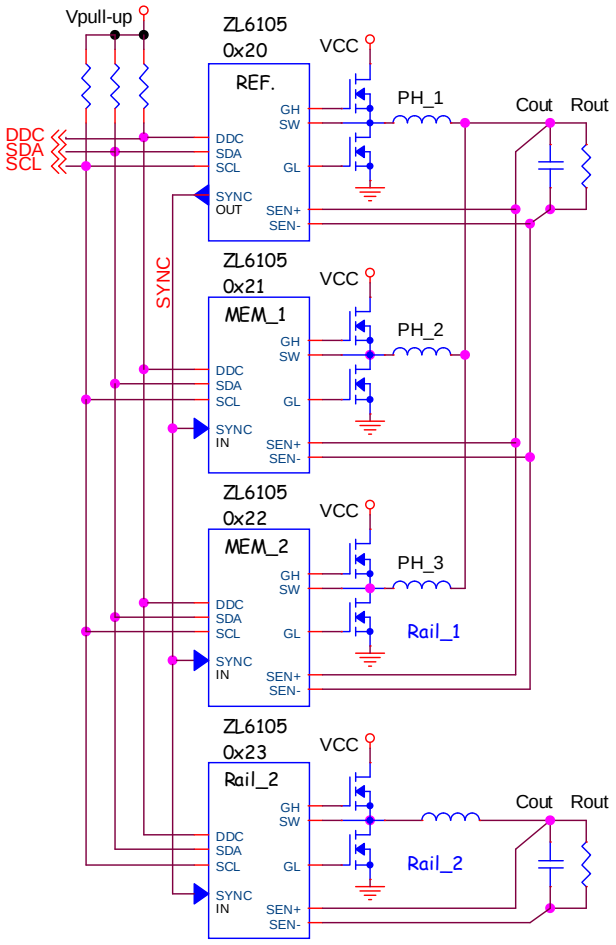

FIGURE 8. EXAMPLE OF SHARING GROUP AND AUXILIARY OUTPUT RAIL WITH A COMMON SYNC CLOCK

Phase Offset

The current sharing group in Figure 8 will autonomously distribute each member’s phase with respect to the SYNC clock. Since the sharing group contains 3 members, each member will be ideally offset in phase by 120°. The actual phase offset is represented by a 4 bit binary number resulting in 16 possible offset values in 22.5° steps. The real phase displacement will be rounded to the closest 22.5° increment. All possible phase displacements are shown in Figure 9.

For the 3-phase example shown in Figure 8. the actual sharing group phase offset will be rounded as shown in Table 3.

TABLE 3. IDEAL vs ACTUAL PHASE OFFSET

PHASE POSITION	IDEAL OFFSET	ACTUAL OFFSET
1	0°	0°
2	120°	112.5°
3	240°	247.5°

Although Rail_2 is connected to the same SYNC clock, it will not be autonomously offset in phase with respect to the current sharing group. Rail_2 will assume an offset of 67.5 degrees from the rising edge of the sync clock based on the configured PMBus address 0x23. Rail_2 can be offset in phase to one of the 16 possible offset values by using the INTERLEAVE command.

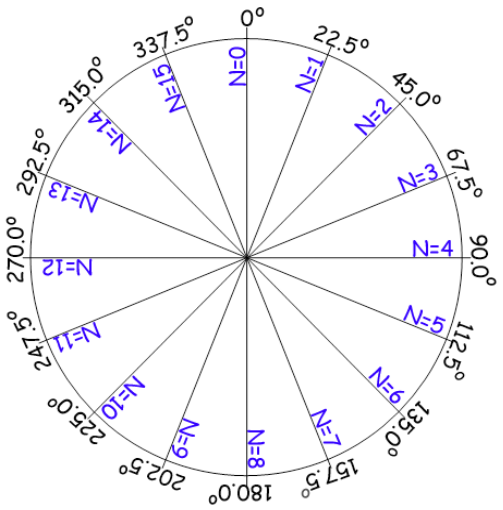

FIGURE 9. PHASE OFFSET RESOLUTION WHEEL

INTERLEAVE Command

Current sharing groups are autonomously offset in phase with respect to each group member, however, when there are multiple sharing groups connected to the same SYNC clock the 2 groups will not autonomously offset from each other. Consider the 2 current sharing groups shown in Figure 10. This configuration consists of 2 output rails with each rail containing a 2-phase sharing group and a common SYNC clock.

After the ISHARE_CONFIG command is configured, each sharing group will autonomously phase spread within the group, but not between the 2 groups. The resulting timing waveform is shown in Figure 11.

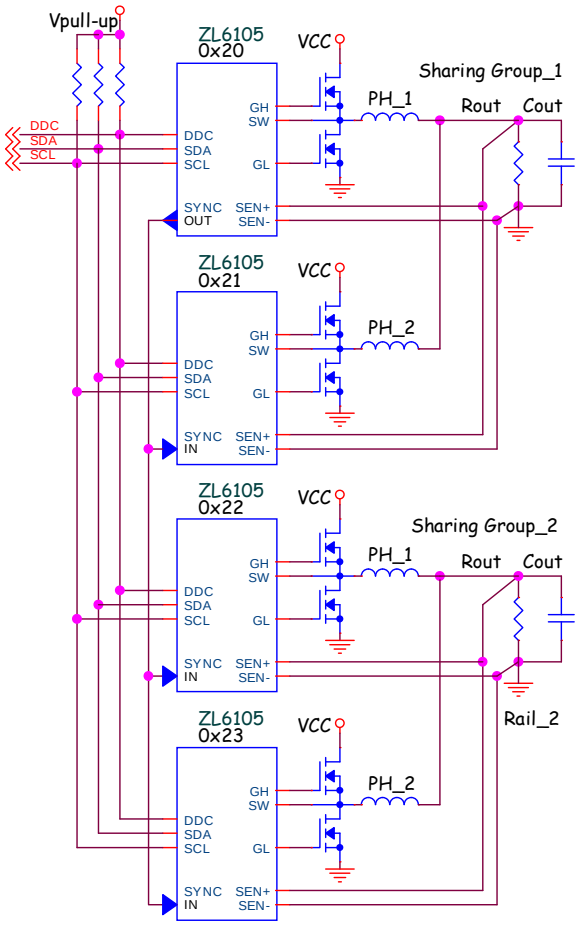

FIGURE 10. EXAMPLE OF 2x2-PHASE CURRENT SHARING GROUPS USING THE SAME SYNC CLOCK

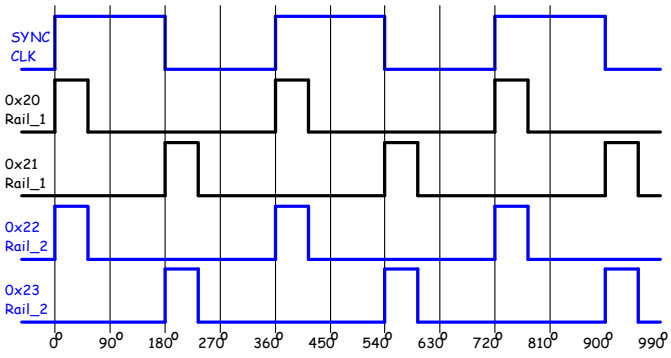

FIGURE 11. TIMING DIAGRAM FOR A 2 RAILx2-PHASE CURRENT SHARING EXAMPLE

Notice that the positional phase equivalents in each sharing group are not offset from each other.

If desired, Sharing Group_2 can be offset in phase from Group_1 by using the INTERLEAVE command field in the GUI or creating an equivalent interleave command line in a configuration file.

The simplest way to achieve equal phase offset for the 4 devices in Figure 10 is to offset Sharing Group_2 by 90°. This is easily done in the GUI by declaring 2 Devices in Sharing Group_2 and assigning the Position in Interleave Group as 4. The INTERLEAVE command would be placed in each config file for Sharing Group_2 with a value of 0x0024.

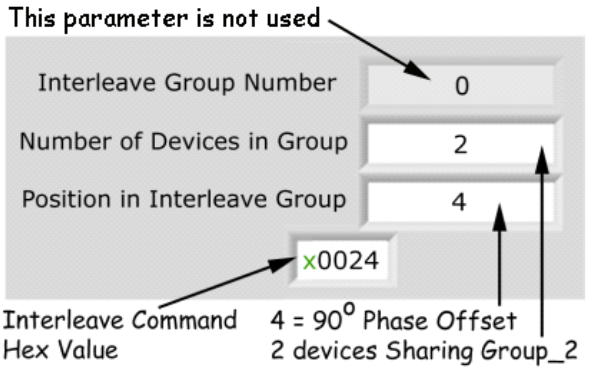

FIGURE 12. INTERLEAVE CONFIGURATION TO OFFSET SHARING GROUP_2 BY 90°

Referencing Figure 9, the value 4 represents an offset of 90°. The same entries are made for both devices in Sharing Group_2's configuration files.

The interleave value for Sharing Group_1 is simply INTERLEAVE = 0000, so the INTERLEAVE command is not used in the configuration files for Sharing Group_1. The Interleave function for Sharing Group 1 is handled by the ISHARE_CONFIG command.

The timing diagram shown in Figure 13 illustrates that each Phase in Sharing Group_2 is now equally offset from Sharing Group_1.

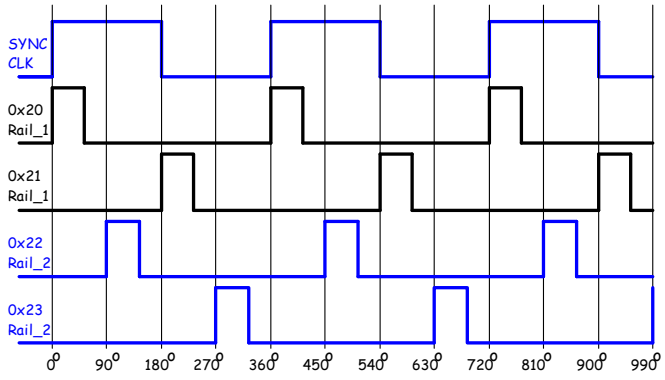

FIGURE 13. 2x2-PHASE CURRENT SHARING GROUPS NOW EQUALLY OFFSET USING INTERLEAVE COMMAND

Ramp Synchronization

During turn-on and turn-off, the voltage ramps of each phase are synchronized to start at the same time. This ensures that inter-phase circulating currents are minimized.

Each current sharing device contains a separate digital controller that executes firmware. The individual controller firmware requires synchronization prior to ramp events to ensure that intra-phase circulating currents are minimized.

This is accomplished by forcing the reference phase to wait at least two additional firmware cycles during ramping events by configuring it to have additional Time On and Time Off Delay relative to the other group members.

When the sharing group receives a hardware or PMBus enable, the member devices initialize their registers and freeze the state of their firmware, once the reference phase completes its extra timing delay it transmits a DDC Ramp Flag and all members of the group produce a sequenced PWM and begin their soft-start routine.

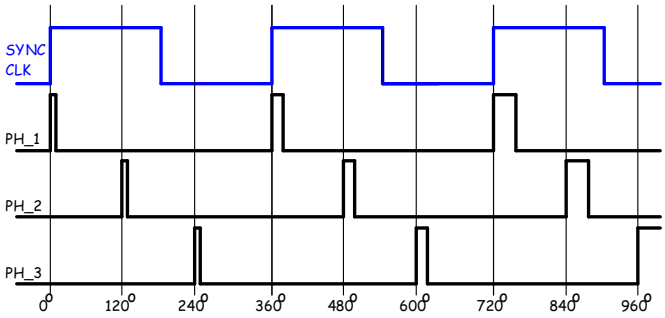

FIGURE 14. START-UP SYNCHRONIZATION

Ensure that the Time On Delay and Time Off Delay parameters for the reference phase are at least 10ms greater than the delay parameters of each member device as shown in Figure 15.

Alternate Ramp Control

Alternate Ramp Control is not supported.

FIGURE 15. SETTING THE REFERENCE TIME ON/OFF DELAYS 10ms GREATER THAN MEMBER DELAYS

Minimum Duty Cycle

Current sharing groups can be comprised of 2 to 7 phases (controllers). Each phase contains its own digital PID controller.

The Minimum Duty Cycle parameter is required when configuring current sharing, enabling a minimum duty cycle ensures that each controller produces an identical initial pulse which helps balance intra-phase currents during ramps. Configure the minimum duty cycle to be slightly above the value specified in the driver data sheet.

The Min Duty Cycle command is located in the USER_CONFIG field on the PMBus Advanced section of the GUI. The ZL8101 contains extra Minimum Duty Cycle options to enable the use of DrMos devices. Reference the ZL8101 data sheet for additional information.

Broadcast Enable/Margin

Broadcast Margin/Enable allows all controllers in a pre-defined group to respond to a single PMBus margin or enable command. The commands can be sent to any SMBus address in the group and all group members will respond relative to their configuration.

PMBus enable and margining commands can be configured with current sharing groups just like single phase converters. The broadcast group can be comprised of current sharing and Single Phase devices. An example is shown in Figure 17.

This configuration contains 3 Single Phase converters (Rails_1-3) and a 3-phase current sharing group (Rail_4). Table 4 shows the DDC_CONFIG and ON_OFF_CONFIG requirements to Enable Broadcast PMBus commands.

To configure a broadcast group, assign each group member the same Broadcast Group Number. The Broadcast Group Number is Part of the DDC_CONFIG command. The ON_OFF_CONFIG parameter has to be set to PMBus Enable.

TABLE 4. BROADCAST MARGIN/ENABLE SETUP

ZL Controller Address	Rail #	Assigned Broadcast Group	ON_OFF_CONFIG	MISC_CONFIG Broadcast Margin/Enable
0x20	1	2	PMBus Enable	Enable
0x21	2	2	PMBus Enable	Enable
0x22	3	2	PMBus Enable	Enable
0x24	4	2	PMBus Enable	Enable
0x25	4	2	PMBus Enable	Enable
0x26	4	2	PMBus Enable	Enable

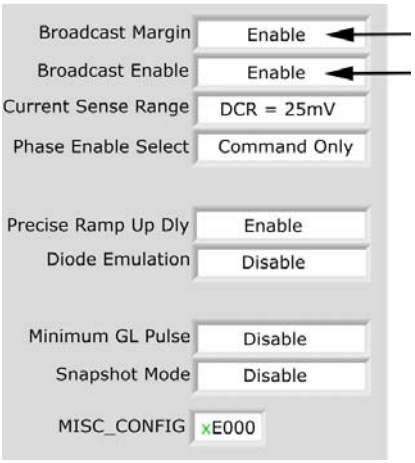

FIGURE 16. SETTING BROADCAST ENABLE AND MARGIN IN THE MISC_CONFIG FIELD

Broadcast Checklist

1. ON_OFF_CONFIG set to PMBus Enable
2. MISC_CONFIG enable broadcast
3. DDC_CONFIG assign Broadcast Group number

After the broadcast group is configured, every member in the group will respond to a PMBus margin or enable command.

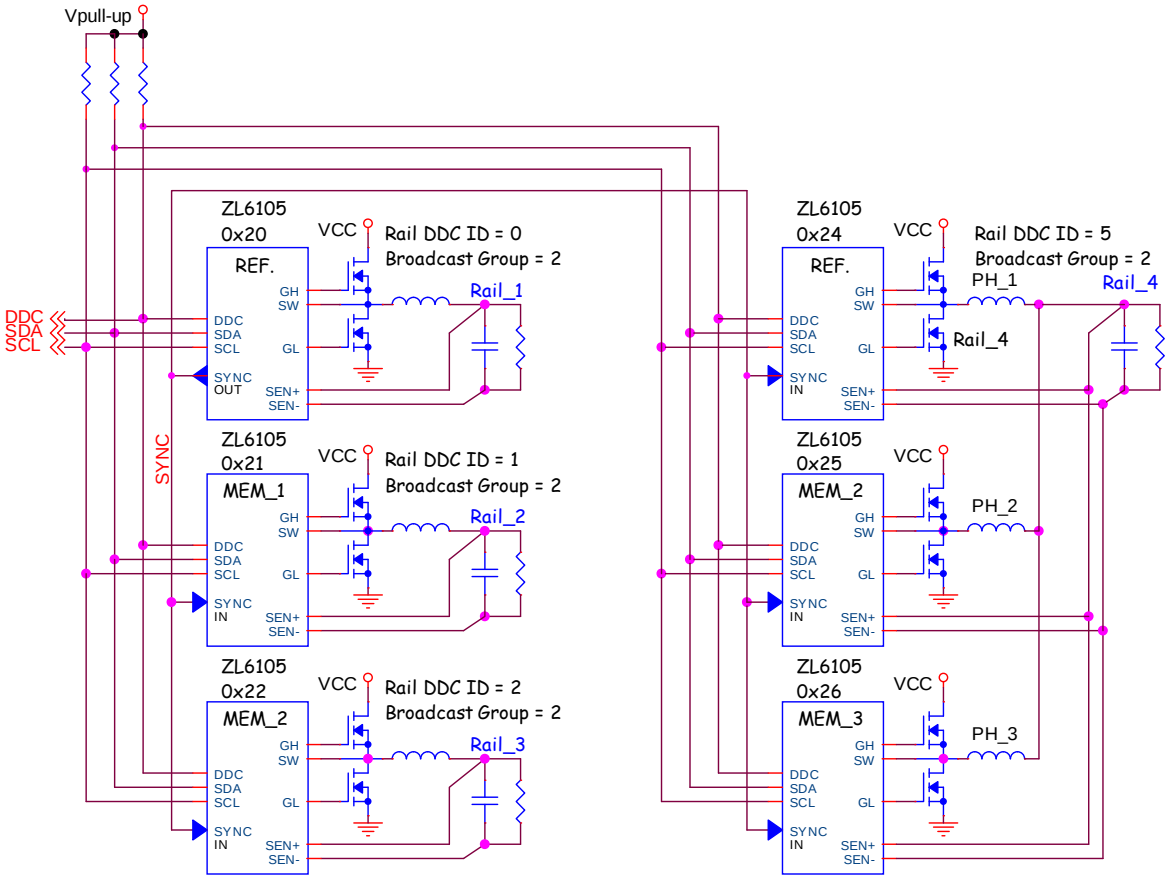

FIGURE 17. 4-RAIL POWER SUPPLY WITH PMBUS BROADCAST MARGIN AND ENABLE

Configuring Current Sharing

Consider the 3-phase current sharing group shown in Figure 18. Ensure that each Zilker Labs device in the group is connected to the same DDC and SMBus. The device with the lowest SMBus address is the designated Reference Phase. The Reference phase is used to provide the load current information to each member device by periodically broadcasting its load current over the DDC Bus. Each member device will trim its reference up or down until the member currents equal the reference current. If the Reference Device is dropped or faults the device with the next lowest PMBus address becomes the new Reference Device.

Rail DDC ID#/ISHARE Rail ID

The Rail DDC ID# is automatically assigned by each controllers firmware and cannot be changed. The Rail DDC ID# is used to configure Fault Spreading and Sequencing for single phase rails. The ISHARE Rail ID is used to configure Fault Spreading and Sequencing for current sharing groups.

The Rail DDC ID is set by the 5 LSB's of the SMBus address. Table 16 (Appendix) maps the Rail DDC ID with the SMBus address. Care must be taken to ensure that duplicate Rail DDC ID's are not created by choosing SMBus address's whose 5 LSB's are identical.

The Rail DDC ID# is not used for current sharing, the ISHARE Rail ID number is used instead, however, versions of the GUI lower than version 4.0 will automatically copy the Rail DDC ID# into the ISHARE Rail ID dialog box, this results in each current sharing controller with a unique ISHARE Rail ID. In order for current sharing to function the ISHARE Rail ID must be the same value for each controller in the sharing group. The ISHARE Rail ID tells the member devices to listen and respond to the load current and DDC events emanating from the reference controller.

The ISHARE Rail ID is part of the ISHARE_CONFIG command. Damage to the controller may result if the current sharing rail is enabled without a common ISHARE Rail ID. The ISHARE_CONFIG command is outlined in Table 2 on page 1.

DDC_CONFIG

The DDC config Field is not used as part of the current sharing algorithm. However, if the current sharing group is part of a broadcast group the Broadcast Group number is assigned in the DDC_CONFIG command.

Table 5 on page 9 shows the format of the DDC_CONFIG command, The Rail DDC ID# field is used to identify the ZL Controller for single phase sequencing and fault spreading. The Rail DDC ID # is described on Page 1 and Table 16 on page 23

TABLE 5.

DDC_CONFIG			
Bits	**Purpose**	**Value**	**Description**
15:13	Reserved	0	Reserved
12:8	Broadcast Group	0 to 31	Group number
7:6	Reserved	0	Reserved
5	DDC TX Inhibit	1	DDC Tranmisson Inhibited
		0	DDC Transmission Enabled
4:0	Rail DDC ID#	0 to 31	DDC ID

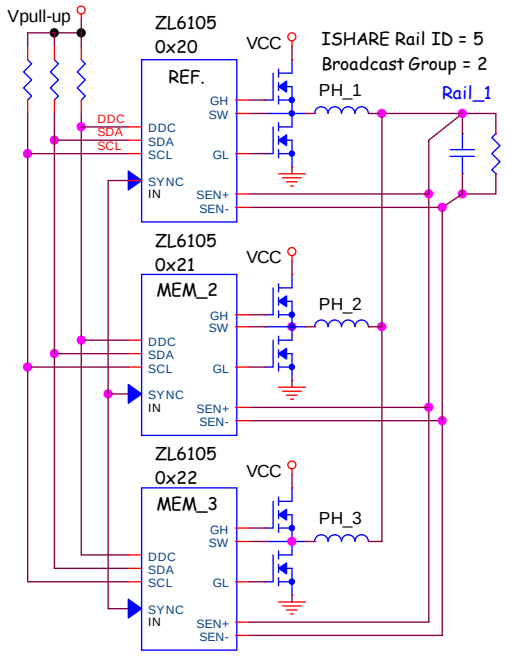

FIGURE 18. 3-PHASE CURRENT SHARING EXAMPLE

ISHARE_CONFIG

The ISHARE_CONFIG field contains 4 fields:

1. **ISHARE Rail ID**
   Assigns the Rail Number for the Current Sharing Group. Must be the same for every controller in a current sharing group. The IShare Rail ID must be configured manually in the configuration file for each sharing group member. Pin-strap current sharing is not supported. The IShare Rail ID is also used to configure Fault Spreading and Sequencing for current sharing groups.
2. **Number of Devices**
   number of devices or phases in current sharing group, this entry is used to calculate phase offset relative to the rising edge of the SYNC Clock.
3. **Device Position**
   This entry is used to calculate phase offset relative to the rising edge of the SYNC Clock.
4. **Current Share Control**
   Enables current sharing, for this example the specific entries for each address is shown in Table 6.

TABLE 6. ISHARE_CONFIG COMMAND CONFIGURATION FOR 3-PHASE CURRENT SHARE EXAMPLE

SMBus Address	ISHARE Rail ID	Number of Devices	Device Position	Phase Displacement Degrees	Current Share Control	ISHARE_CONFIG Hex
0x20	5	3	1	0	Enabled	0x541
0x21	5	3	2	120	Enabled	0x545
0x22	5	3	3	240	Enabled	0x549

USER_CONFIG

The following parameters related to current sharing is located in the USER_CONFIG field and must be set to properly configure current sharing.

Min Duty Cycle

The minimum allowable duty cycle must be set to Enable, to ensure that each phase starts the turn-on ramp with the same pulse width, without missing pulses. The Min Duty Cycle function is equal to:

$$inDutyCycle = N \times \frac{TSW}{256} \quad \text{(EQ. 2)}$$

TSW = Switching Frequency Period

TABLE 7.

MIN DUTY CYCLE N OPTIONS	
DEVICE	**N**
ZL6105	1-4
ZL8101	0, 2, 4, 6, 8, 10, 12, 14

The Min Duty Cycle function is also used to ensure that PWM pulses below the minimum are not presented to an external driver or DrMos device. The Minimum Duty Cycle value should be set equal to or slightly above the driver requirement.

SYNC Time-out Enable

The SYNC Time-out Enable function is used to configure the state of the SYNC output when the controller is disabled. If the controller is supplying the SYNC signal in a current sharing group, SYNC Time-out must be set to SYNC always On. This will ensure that the SYNC source is ready prior to rail enable. Always on also ensures that if the SYNC source is dropped from the current sharing group that the SYNC clock will remain present to the standing group members.

The Reference Controller is typically used to provide the SYNC Clock. However any device internal or external to the sharing group can provide the SYNC Clock.

SYNC Input Mode/SYNC Pin Configuration

The SYNC Input Mode is used along with the SYNC Pin Configure parameter to specify whether the device will output the SYNC clock or use the SYNC clock as an input.

SYNC Clock Source Mode (device is outputting Sync): Set SYNC Input Mode to Pinstrap Input and set SYNC Pin Configure to Output Int. Signal. The controller will now operate as a clock source.

SYNC Clock Input Mode (device is using an external Sync): Configure SYNC Input Mode to External Sync now the controller will use the SYNC signal present on its Sync Pin.

Configure the SYNC Output Mode command in the MFR_CONFIG field to be Push-Pull or Open Drain to satisfy your system design requirements. Reference the device data sheet for additional information.

Standby Mode

Standby Mode is used to select whether the controller is in Low Power mode or Monitor Mode. Low Power Mode is not available with current sharing groups. All current sharing controllers must me configured as monitor mode.

Standby mode must be set to Monitor Enabled for both Reference and Member Devices. Setting this parameter to monitor mode ensures that the firmware is initialized prior to enabling the output rail.

The other entries in the USER_CONFIG field do not affect current sharing groups, and should be configured to meet the designer's system requirements. For additional information about these parameters please reference.

Lowside FET Mode

The Lowside FET Mode is used to configure the state of the lowside FET when the Rail or controller is disabled. The default mode is Off when Disabled. This means that the lowside gate is held low (FET off) when the controller is disabled. The FET on mode is used to mimic an active crowbar during an over-voltage condition, or to discharge a pre-bias leakage.

The **USER_CONFIG** GUI entries for this example are shown in Figure 19, illustrating the configuration for the Reference device. Figure 20 illustrates the configuration for Member device(s).

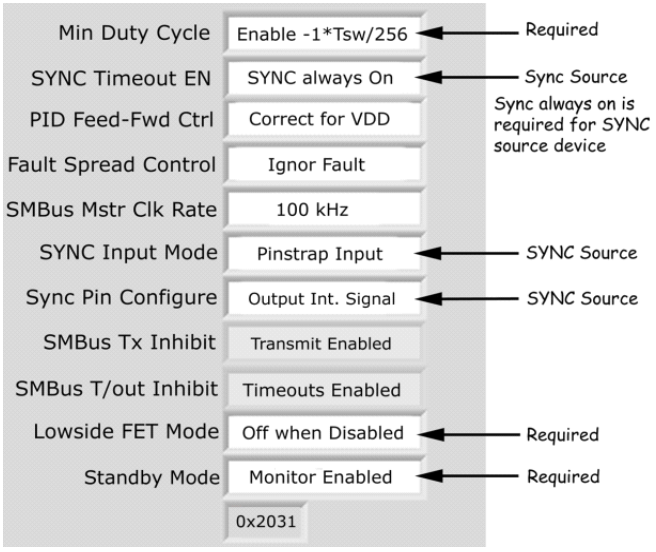

FIGURE 19. USER_CONFIG FIELD (REFERENCE)

Reference AN2026 "PowerNavigator™ Users Manual" and AN2033 "Zilker Labs PMBus Command Set for DDC Products" for additional information.

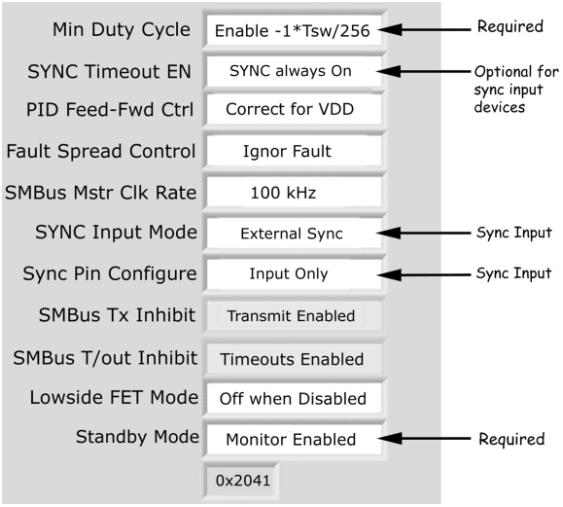

FIGURE 20. USER_CONFIG FIELD (MEMBER)

MFR_CONFIG

The following parameters related to current sharing is located in the MFR_CONFIG field and must be set to properly configure current sharing.

I Sense Delay

The I Sense Delay parameter is used to configure the time that current samples are ignored after FET switch transitions. The delay parameter is configured to be greater than the worst case switch node ring out time. Ensure that the same blanking value is used for the Reference and Member device(s).

I Sense Control

I Sense Control is used to configure the current sensing method. Various modes of current sensing are available depending on duty cycle and switching frequency. Current sensing options are shown below in Table 8. A lumped or distributed resistor can be substituted for $r_{DS(ON)}$ and DCR sensing. Ensure that the same I Sense Control is used for the Reference and Member device(s).

TABLE 8. CURRENT SENSING METHOD SELECTION

CURRENT SENSE CONTROL	USAGE
Ground referenced, down-slope ($r_{DS(ON)}$)	Low duty cycle and low F_{SW} Not supported on the ZL8101
V_{OUT} referenced, down-slope (Inductor DCR Sensing)	Low duty cycle and high F_{SW}
V_{OUT} referenced, up-slope (Inductor DCR sensing)	High duty cycle

NLR During Ramp

Determines if NLR is active during ramps or waits until Power-Good is asserted. This should always be set to **Wait for PG** for both Reference and Member device(s) when configuring current sharing groups.

Alternate Ramp Control

Set to disable for Reference and Member device(s). Alternate Ramp control is not supported for the controllers referenced in this document.

SYNC Output Mode

Configures the SYNC pin as Open Drain or Push-Pull. SYNC Output Mode is typically set to Push-Pull for the SYNC clock source and Open Drain for devices that receive the SYNC clock as an input.

The MFR_CONFIG GUI entries are shown below. The comments refer to current sharing groups. Reference AN2026 "PowerNavigator™ Users Manual" for additional information.

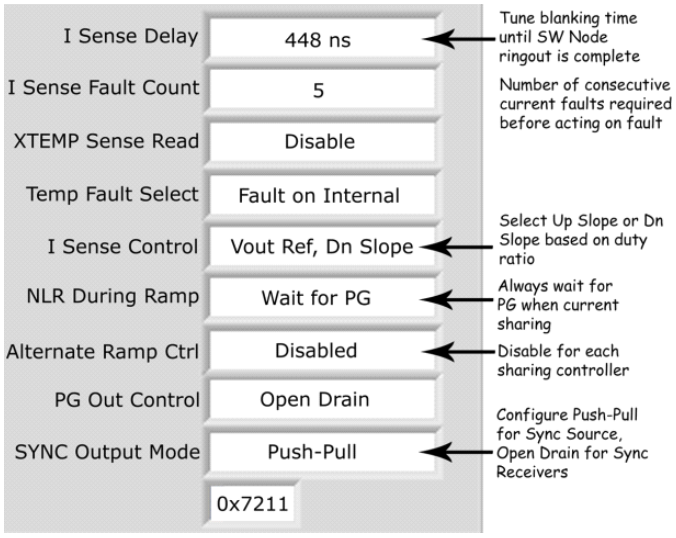

FIGURE 21. MFR_CONFIG FIELD

TEMPCO_CONFIG

The TEMPCO_CONFIG command is used to configure the temperature correction factor and temperature measurement source (internal or external) when performing temperature coefficient correction for the current sensing element. TEMPCO_CONFIG values are applied as a negative correction to a positive temperature coefficient. The TEMPCO_CONFIG command is defined in Table 9. The TEMPCO_CONFIG parameter must be configured to the same value for the Reference and Member(s).

TABLE 9. TEMPO_CONFIG

FIELD	PURPOSE	VALUE	DESCRIPTION
7	Selects the temperature sensor source for tempco correction	0	Selects the internal temperature sensor
		1	Selects the XTEMP pin for temperature measurements
6:0	Sets Tempco correction in units of 100ppm/°C	TC	$R_{SEN(EXT)}$
			$R_{SEN(INT)}$

Equation 3 can be used to fine tune the temperature correction for internal and external sense elements.

$$R_{SEN(EXT)} = IOUT\_CAL\_GAIN \times (1 + TC \times 10^{-4} \times (T - 25))$$
$$R_{SEN(INT)} = IOUT\_CAL\_OFFSET \times (1 + TC \times 10^{-4} \times (T - 25)) \quad \text{(EQ. 3)}$$

Where:

IOUT_CAL_GAIN = the impedance of the current sense element at +25°C

IOUT_CAL_OFFSET = offset added to IOUT readings, this offset is used to compensate for current measurement error due to blanking.

$R_{SEN(EXT)}$ = DCR inductor resistance

$R_{SEN(INT)}$ = Internal silicon temp diode

$r_{DS(ON)}$ = Low-side FET channel resistance

T = Temperature measured by sensing device

TC = Temperature correction factor

The hex values in Table 10 can be used to accurately compensate most designs if the measurement element is tightly (thermally) coupled to the sense element.

TABLE 10. TYPICAL TEMPCO_CONFIG VALUES BY ZL PART NUMBER

ZL DEVICE	EXTERNAL TEMP DIODE	INTERNAL SILICON DIODE
ZL6105	A8	2C
ZL8101	A8	2C

AUTOCOMP_CONFIG

The ZL6105 and ZL8101 have an auto compensation feature that measures the characteristics of the power train and calculates the proper compensator PID coefficients. Auto compensation is configured using the FC0 and FC1 pins, GUI, or config files, reference the specific product data sheets for additional information.

When configuring current sharing groups to use autocomp, every device in the sharing group must have the same AUTOCOMP_CONFIG value.

When the Auto Compensation algorithm is enabled, the configured soft-start values (Rise/Fall times) are used to calculate the loop gain that's used during the turn-on/turn-off ramps to ensure current sharing while ramping. If the rise/fall time is set too large the gain term cannot be optimized to ensure current balance during ramping. To ensure current balance constrain current sharing groups to rise/fall times between 5ms and 20ms.

While ramping, the loop bandwidth is intentionally set to a very low value so transient compliance will be very poor. The designer should limit dynamic loading while ramping. Even if autocomp is disabled and the sharing group employs a user defined compensator, transient response will be poor during ramps.

Once the ramp has completed, the autocomp algorithm will begin and a new optimized compensator solution will be found and the compensator solution will transmit over the DDC Bus such that each controller has the same PID compensator values.

If Autocomp is disabled the controllers will switch to the configured compensator by using the PID Taps defined in the configuration files.

If Auto Comp is enabled, V_{IN} must be stable before the autocomp algorithm begins, as shown in Equation 4.

$$\frac{\Delta Vin}{Vin_{NOM}}\% \leq \frac{100\%}{1+\frac{256\times Vout}{Vin_{NOM}}} \quad \text{(EQ. 4)}$$

AUTO_COMP_CONFIG

The AUTO_COMP_CONFIG command is used to configure auto compensation.

AUTO COMP ENABLE

Used to enable/disable autocomp and determine how often the rail runs the autocomp algorithm. The choices are:

- Autocomp once, will run autocomp algorithm each time the rail is enabled
- Autocomp every second will initiate a new autocomp algorithm each 1 second
- Autocomp every minute will initiate a new autocomp algorithm every minute.

It is recommended that current sharing groups use only the Autocomp Once option.

AUTO COMP STORE

controls whether or not the autocomp result is stored in ram. If autocomp store is enabled, the autocomp result found on the first ramp will be used on all subsequent ramps, as long as input power to the controller is present. If input power is cycled, the result will be lost. Autocomp Store disabled will run a new autocomp algorithm the first time the rail is enabled.

POWER-GOOD ASSERT

If the PG Assert parameter is set to "Use **PG Delay"**, PG will be asserted according to the POWER_GOOD_DELAY command, after which Auto Comp will begin. When Auto Comp is enabled, the user must not program a Power-Good Delay that will expire before the ramp is finished. If PG Assert is set to **"IMM After AC"**, PG will be asserted immediately after the first Auto Comp cycle completes and the configured POWER_GOOD_DELAY parameter will be ignored. Since the Autocomp algorithm typically takes between 50ms and 200ms to complete the option **"IMM After AC"** is suggested.

AUTO COMP GAIN

The Auto Comp Gain control scales the Auto Comp results to allow a trade-off between transient response and steady-state duty cycle jitter. A setting of 100% will provide the fastest transient response while a setting of 10% will produce the lowest jitter. The optimal gain value will need to be determined empirically based on the system requirements.

PMBus Basic Commands

VOUT_COMMAND

Set each current sharing phase to the same output voltage value.

The VOUT_COMMAND can be stated in each configuration file, or VOUT_COMMAND can be defined by pinstrap. If using pinstraps to configure the current sharing rail voltage, don't use the VOUT_COMMAND statement in the configuration files.

VOUT_TRIM

Typically set to 0 (default value) for each current sharing phase. The reference phase will always retain a zero value. Member phases will adjust the trim value until all phases carry equal load current. If an offset voltage is desirable to overcome the effects of droop use the VOUT_CAL_OFFSET command to add an offset. See "(VOUT_CAL_OFFSET)". The VOUT_TRIM command is not available when current sharing.

VOUT_CAL_OFFSET

The VOUT_CAL_OFFSET command is used to apply an offset voltage that can compensate for the load-line droop. While positive and negative offset values are valid, a positive offset value is typically used with a magnitude of Equation 5.

$$VOUT\_CAL\_OFFSET = 0.5\times I_{MAX}\times R_{DROOP} \quad \text{(EQ. 5)}$$

If the VOUT_CAL_OFFSET command is used, ensure that each group member is assigned the same VOUT_CAL_OFFSET value.

VOUT_DROOP

Droop resistance is used as part of the current sharing algorithm. The recommended droop or loadline resistance for current sharing groups is between 0.15mΩ and 1.0mΩ. Each group member is assigned the same droop value.

MAX_DUTY

The maximum duty cycle must be constrained as the switching frequency increases. Configure the MAX_DUTY cycle to a maximum value for each group member per Equation 6, round the result down to the closest integer value. Table 11 lists MAX_DUTY values for a few common switching frequencies.

$$\delta\max(\%) = [1-(150ns\times Fsw)]\times 100 \quad \text{(EQ. 6)}$$

TABLE 11. MAX_DUTY VALUES FOR COMMON SWITCHING FREQUENCIES

FSW (kHz)	MAX DUTY (%)
200	97
400	94
600	91
800	88
1000	85
1400	80

TON_DELAY, TOFF_DELAY

Time On Delay and Time Off Delay parameters for the reference phase must be set at least 10ms greater than the delay parameters of each member device, reference Figure 15.

ADAPTIVE DEADTIME

The ZL6105 and ZL8101 controllers utilize a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the top and bottom FETs. When enabled the algorithm continuously adjusts the deadtimes until the duty cycle reaches a minimum.

When current sharing several other algorithms are also running I.E. local droop, rail droop, voltage regulation, and current balance algorithms. In order to avoid the possibility of these algorithms interacting with each other, the adaptive deadtime algorithm must be disabled while current sharing, set deadtimes to Freeze and then configure fixed deadtimes to optimize the selected drive train.

To configure the deadtimes for current sharing use the DEADTIME_CONFIG command. The DEADTIME _CONFIG command structure is shown Table 12.

TABLE 12.

DEADTIME_CONFIG			
BITS	PURPOSE	VALUE	DESCRIPTION
15	Sets high to low deadtime mode	0	Adaptive H-to-L control
		1	Freeze H-to-L deadtime
14:8	Sets H-to-L deadtime	H	H X 2ns (signed)
7	Sets L-to-H deadtime mode	0	Adaptive L-to-H control
		1	Freeze L-to-H deadtime
6:0	Sets H-to-L deadtime	L	H X 2ns (signed)

There are 2 other commands associated with deadtimes, DEADTIME_MAX and DEADTIME. When the deadtimes are set to Freeze mode these commands are not needed, simply omit them from the configuration file.

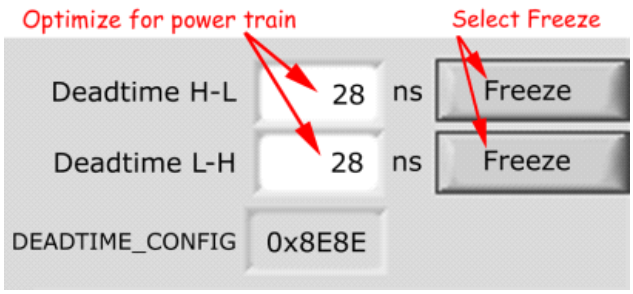

FIGURE 22. RECOMMENDED DEADTIME CONFIGURATION

Voltage Tracking

The ZL8101 integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no extra components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the member device's output regulation.

Voltage tracking for current sharing groups is the same for single rail designs with the exception that a configuration file or PMBus operation is required. Pin-strapped current share tracking is not supported.

The ZL6105 and ZL8101 offer two modes of tracking: coincident and ratiometric. Figures 23 and 24 illustrate the output voltages for the two tracking modes.

1. *Coincident*. This mode configures the controller to ramp its output voltage at the same rate as the voltage applied to the VTRK pin. Two options are available for this mode;
   - Track at 100% VOUT limited. Member rail tracks the reference rail and stops when the member reaches its configured target voltage. Figure 23A and 23B.
   - Track at 100% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin. Figure 23C.

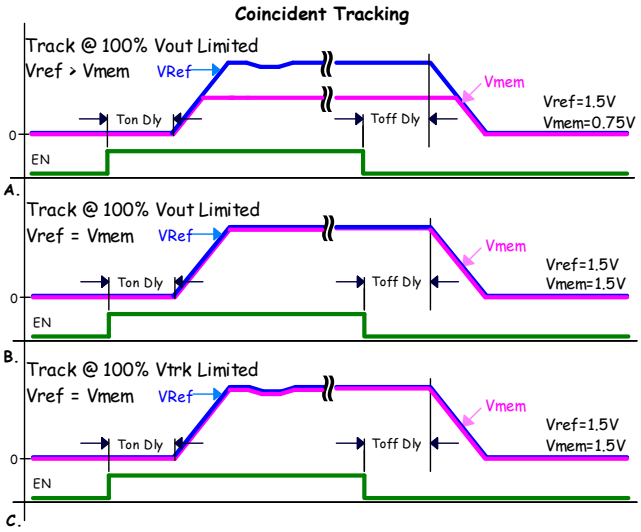

FIGURE 23. COINCIDENT TRACKING

2. *Ratiometric*. This mode configures the controller to ramp its output voltage as a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor maybe used to configure a different tracking ratio.
   - Track at 50% VOUT limited. Member rail tracks the reference rail and stops when the member reaches 50% of the reference's target voltage
   - Track at 50% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin until the member rail reaches 50% of the reference rail voltage, or if the member is configured to less than 50% of the reference the member will achieve its configured target

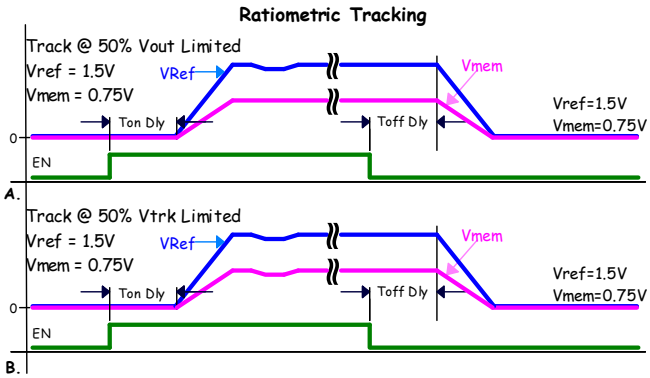

FIGURE 24. RATIOMETRIC TRACKING

Tracking with Autocomp

The ZL6105 and ZL8101 uses a unique ramping algorithm that results in near perfect tracking while ramping. This is accomplished by deriving different compensator coefficients for ramping than those used for steady-state operation. The ramp compensation is derived from the configured rise/fall time, VIN, and VOUT. While ramping the loop bandwidth is intentionally set to a very low value so to ensure that inter-phase current balance is maintained. Since the loop bandwidth is low response to transients will be limited. The user should limit dynamic loading while ramping. Once the ramp has completed the autocomp algorithm will begin and a new optimized compensator solution will be found. If Autocomp is disabled the controllers will switch to the configured compensator by using the PID Taps defined in the configuration files. If Autocomp is enabled the tracking member Rise/Fall times might need to be adjusted slightly until the desired tracking accuracy is achieved. For the best possible tracking accuracy disable autocomp and manually assign PID coefficients in the configuration file. Even though Autocomp is disabled current sharing groups will still us a calculated ramping compensator that ensures current balance.

Current Sharing and Tracking

When the ZL6105 and ZL8101 is configured in a current sharing group and voltage tracking is desired, the VTRK pin of each sharing group member must be tied together, and connected to the reference rails output voltage. Figures 25 and 26 show tracking connections for current sharing groups. Two current sharing groups can also be configured to track each other.

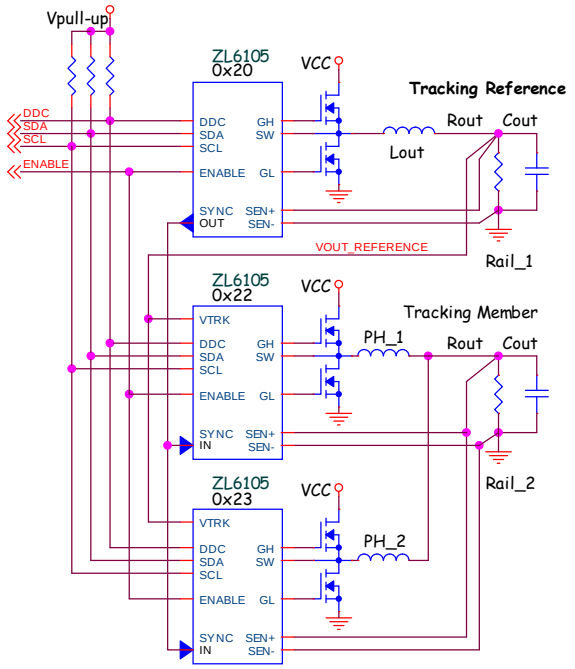

FIGURE 25. CURRENT SHARING GROUP TRACKING A SINGLE RAIL

Configuring Tracking with Current Sharing

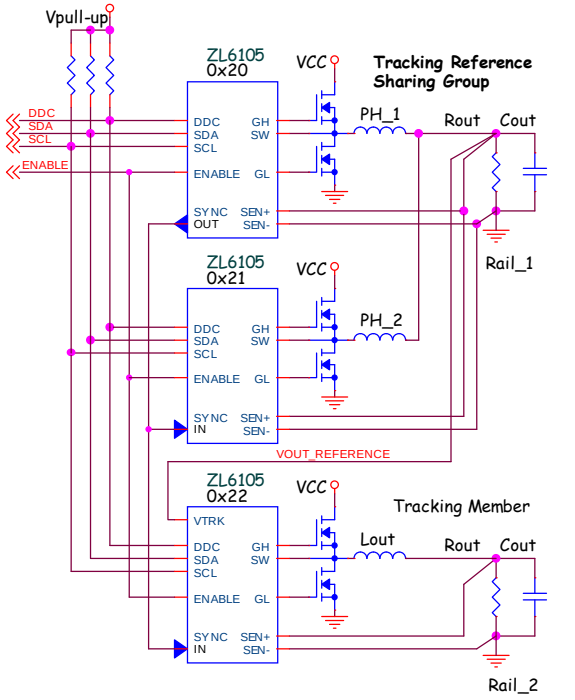

FIGURE 26. SINGLE RAIL TRACKING A CURRENT SHARING GROUP

In a tracking group, the rail output with highest voltage is defined as the reference device. The device(s) that track the reference is called member device(s). The reference device will control the ramp delay and ramp rate of all tracking devices and is not placed in the tracking mode. The reference device is configured to the highest output voltage for the group and all other device(s)

output voltages are meant to track and never exceed the reference device output voltage. The reference device must be configured to have a minimum Time-On Delay as shown in Equation 7.

$$t_{OnDly}(REF) \geq t_{OnDly}(MEM) + t_{OnRise}(REF) + 5ms \quad \text{(EQ. 7)}$$

The member device(s) must be configured to have a minimum Time-Off Delay as shown in Equation 8.

$$t_{OffDly}(MEM) \geq t_{OffDly}(REF) + t_{OffFall}(REF) + 5ms \quad \text{(EQ. 8)}$$

When the Tracking Reference is comprised of a current sharing group the delay time must me added to the standing current sharing t_{OnDly}. Using Figure 26 as an example the non-Tracking timing configuration is shown below in Table 13.

TABLE 13. NON-TRACKING DELAY TIMING FOR FIGURE 26

RAIL #	V_{OUT} (V)	t_{ON_DLY} (ms)	t_{ON_RISE} (ms)	t_{OFF_DLY} (ms)	t_{OFF_FALL} (ms)	MODE
Rail_1 Tracking Reference	1.5	5	5	5	5	Tracking Disabled
Rail_2 Sharing Reference Tracking Member	0.75	15	5	5	5	Tracking Disabled
Rail_2 Sharing Member Tracking Member	0.75	15	5	15	5	Tracking Disabled

To obtain the tracking timing we get the following

$$t_{OnDly}(Ref) = 15ms + 5ms + 5ms = 25ms \quad \text{(EQ. 9)}$$

$$t_{OffDly}(Mem) = 5ms + 5ms + 5ms + 15ms = 30ms \quad \text{(EQ. 10)}$$

The Tracking Timing is shown below in Table 14.

TABLE 14. TRACKING TIMING FOR FIGURE 26

RAIL #	V_{OUT} (V)	t_{ON_DLY} (ms)	t_{ON_RISE} (ms)	t_{OFF_DLY} (ms)	t_{OFF_FALL} (ms)	MODE
Rail_1 Tracking Reference	1.5	25	5		5	Tracking Disabled
Rail_2 Sharing Reference Tracking Member	0.75	15	5	5	5	Track at 100% V_{OUT} or V_{TRAK} Limited
Rail_2 Sharing Member Tracking Member	0.75		5	30	5	Track at 100% V_{OUT} or V_{TRAK} Limited

All of the ENABLE pins must be connected together and driven by a single logic source. If PMBus ENABLE is going to be used ensure that the tracking and sharing devices are configured to be in the same Broadcast Group with the DDC_CONFIG command. Ensure that Broadcast Enable is active for each controller in the tracking and sharing group, Broadcast Enable is part of the MISC_CONFIG command.

Compensation

The ZL6105 and ZL8101 Digital DC/DC PWM Controllers include an auto compensation algorithm. The auto compensation function can be used to find a compensator each time the current sharing rail is enabled or the algorithm can be used to find a suitable compensator which can be inserted in each configuration file.

Autocomp every second and autocomp every minute should not be selected with current sharing groups.

The Zilker Labs CompZL program can be used to obtain PID taps that ensure stability and result in moderate to optimal transient response.

Filter Design

The design of the output filter is based on the system requirements for ripple, noise, transient response, and phase-count.

After the filter design is complete, consider any one of the phases for the compensation analysis and divide the total capacitance by the number of phases. The resultant filter consists of the phase output inductor and the equivalent phase capacitance. Consider the 3-Phase example shown in Figure 27. This schematic is drawn symmetrically with identical phase filters; consider any one of the phases plus any common output capacitance divided by the number of phases, in this case 3.

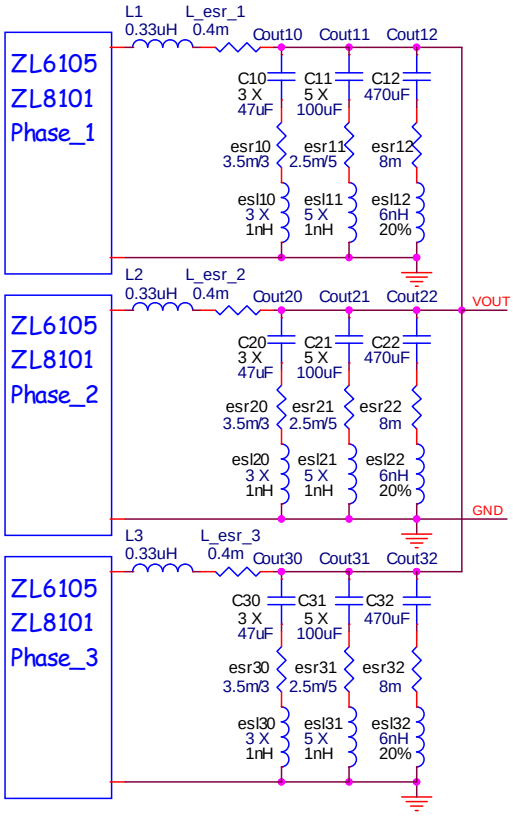

FIGURE 27. 3-PHASE CURRENT SHARING EXAMPLE

The resultant 3-Phase compensation model reduces to the configuration shown in Figure 28.

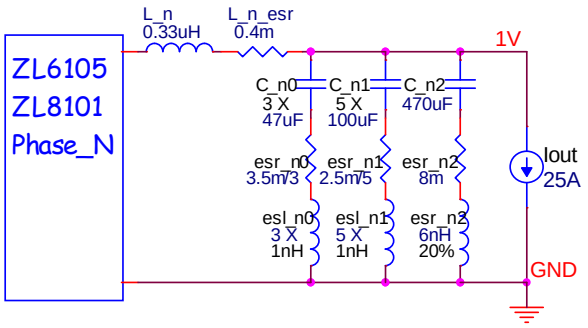

FIGURE 28. CURRENT SHARING COMPENSATION MODEL (USING COMPZL TO CALCULATE TAPS)

Using CompAZL to Calculate Taps

In order to calculate accurate taps for the sharing group, all of the conversion losses need to be identified and entered into the CompZL power stage model. These losses include inductor AC loss, routing loss, and FET switching loss.

It is particularly important to identify and estimate these losses with low impedance (hi Q) output filters. These previously unaccounted losses in the CompZL program increase the filter damping and usually enable the use of real zeros in the compensator.

Real zeros can be strategically placed above and below the filter resonant frequency and result in increased midband frequency gain. Please reference AN2035 for additional information on using CompZL.

Equations 11 through 17 can be used to estimate the conversion losses that are not included in CompZL, including these losses in the analysis increases circuit damping and the effectiveness of using real zeros. Once the analysis is complete, simply substitute the calculated value R_{DCR}' into the CompZL model for DCR.

R_{DCR}' is calculated by subtracting the losses known by CompZL from the total circuit losses. The total losses are known by measuring, calculating, or estimating the conversion efficiency at the operating point of interest. Once the efficiency is known, these equations (Equations 11 through 17) can be used to obtain the losses not considered in the CompZL program at the operating point of interest.

$$R_{DCR}' = \frac{P_{IN} - P_{HI\_Cond} - P_{LO\_Cond} - P_{LOUT} - P_{OUT}}{I_{OUT}^2} \quad \text{(EQ. 11)}$$

$$P_{IN} = \left(\frac{P_{OUT}}{\eta} - V_{IN} * I_{QC} \right) \quad \text{(EQ. 12)}$$

$$P_{HI\_Cond} = I_{OUT}^2 * R_{DS\_HI} * \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 13)}$$

$$P_{LO\_Cond} = \left(I_{OUT}^2 * R_{DS\_LO} \right) * \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad \text{(EQ. 14)}$$

$$P_{LOUT} = I_{LOUT}^2 * R_{DCR} \quad \text{(EQ. 15)}$$

$$P_{OUT} = V_{OUT} * I_{OUT} \quad \text{(EQ. 16)}$$

$$I_{LOUT} = \sqrt{I_{OUT}^2 + \frac{\left[\left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times V_{OUT} \right]^2}{L_{OUT} \times F_{SW}}}{12} \quad \text{(EQ. 17)}$$

Where:

R_{DCR}' = Total resistive conversion loss minus CompZL calculated losses

P_{IN} = Total input power

P_{HI_Cond} = High-side FET Conduction loss

P_{LO_Cond} = Low-side FET Conduction loss

P_{LOUT} = Output inductor DCR loss

I_{OUT}^2 = Output current

R_{DS_LO} = Low-Side FET $r_{DS(ON)}$

R_{DS_HI} = High-Side FET $r_{DS(ON)}$

η = Converter efficiency

V_{IN} = Converter input voltage

V_{OUT} = Converter output voltage

I_{QC} = Controller quiescent current

I_{OUT} = Converter output current

I_{LOUT} = Output inductor RMS current

Compensation Example

The 3-Phase converter shown in Figure 28 has the following component values:

V_{OUT} = 1.0V

V_{IN} = 12V

I_{OUT} = 25A/Phase

F_{SW} = 615kHz/Phase

C_{OUT_n0} = 3 X 47µF, 3.5mΩ, 1nH

C_{OUT_n1} = 5 X 100µF, 2.5mΩ, 6nH

C_{OUT_n2} = 470µF, 8mΩ, 6nH

L_{OUT} = 0.33µH

DCR = 0.4mΩ

R_{DS_HI} = 4mΩ

R_{DS_LO} = 2mΩ

ç = 85%

I_{QC} = 35mA

The individual power losses are calculated in Equations 18 through 23. The losses already accounted for in CompZL are then subtracted from the input power.

$$P_{IN} = \left(\frac{1V * 25A}{0.84} - 12V * 35mA \right) = 28.99W \quad \text{(EQ. 18)}$$

$$P_{HI\_COND} = 25^2 A * 4m\Omega * \frac{1V}{12V} = 0.208W \quad \text{(EQ. 19)}$$

$$P_{LO\_COND} = 25^2 A * 2m\Omega * \left(1 - \frac{1V}{12V} \right) = 1.15W \quad \text{(EQ. 20)}$$

$$I_{LOUT} = \sqrt{25^2 A + \frac{\left[\frac{\left(1 - \frac{1V}{12V} \right) * 1V}{0.33uH * 615KHz} \right]^2}{12}} = 25.03A \quad \text{(EQ. 21)}$$

$$P_{LOUT} = 25.03^2 A * 0.4m\Omega = 0.25W \quad \text{(EQ. 22)}$$

$$P_{OUT} = 1V * 25A = 25W \quad \text{(EQ. 23)}$$

$$R'_{DCR} = \frac{29.34W - 0.204W - 1.145W - 0.25W - 25W}{25^2 A} = 3.82m\Omega \quad \text{(EQ. 24)}$$

The adjusted value of R'_{DCR} is 3.82mΩ. Type this value into the CompZL location for the inductor DCR. This adjusted value now contains all of the frequency dependent losses at the operating point of interest, these losses were previously unaccounted for in the CompZL model.

This new adjusted value yields a more accurate compensation model and increases the filter dampening. As a result, the possibility of using real zeros increases with low impedance output filters.

Suggested Guidelines

To ensure that the digital PID controller constrains internal noise and minimizes PWM jitter, the low frequency gain Gc should be constrained to 30dB if possible. Q should be initially set between 0.1 to 0.4. The compensator should be set to Overdamped (real zeros). If the Q of the output filter is extremely low, (very small parasitic resistance) an overdamped compensator will not be possible. In that case switch to the underdamped mode.

The compensator natural frequency Fn is adjusted below the calculated output filter natural frequency (see Equation 25), by moving the zeros until the phase margin, gain margin, and crossover criteria is met.

The compensation results are shown in Figure 29. the compensator is set to overdamped (real zeros). The gain term was set to initially 25dB, and Q was set to 0.35.

$$Fn = \frac{1}{2 * \pi * \sqrt{Lout * Cout}}$$

$$Fn = \frac{1}{2 * \pi * \sqrt{0.33uH * 1111uF}} = 8.31kHz \quad \text{(EQ. 25)}$$

While moving each zero in turn, observe the actual phase and gain margin values and ensure that the phase and gain margin goals are met.

Notice how the gain levels off at approximately 2.5kHz. This is due to the careful placement of the zeros and results in a flattened midband gain characteristic with improved damping and transient response.

Once the PID coefficients have been calculated, enter the same values for each phase in their respective configuration files.

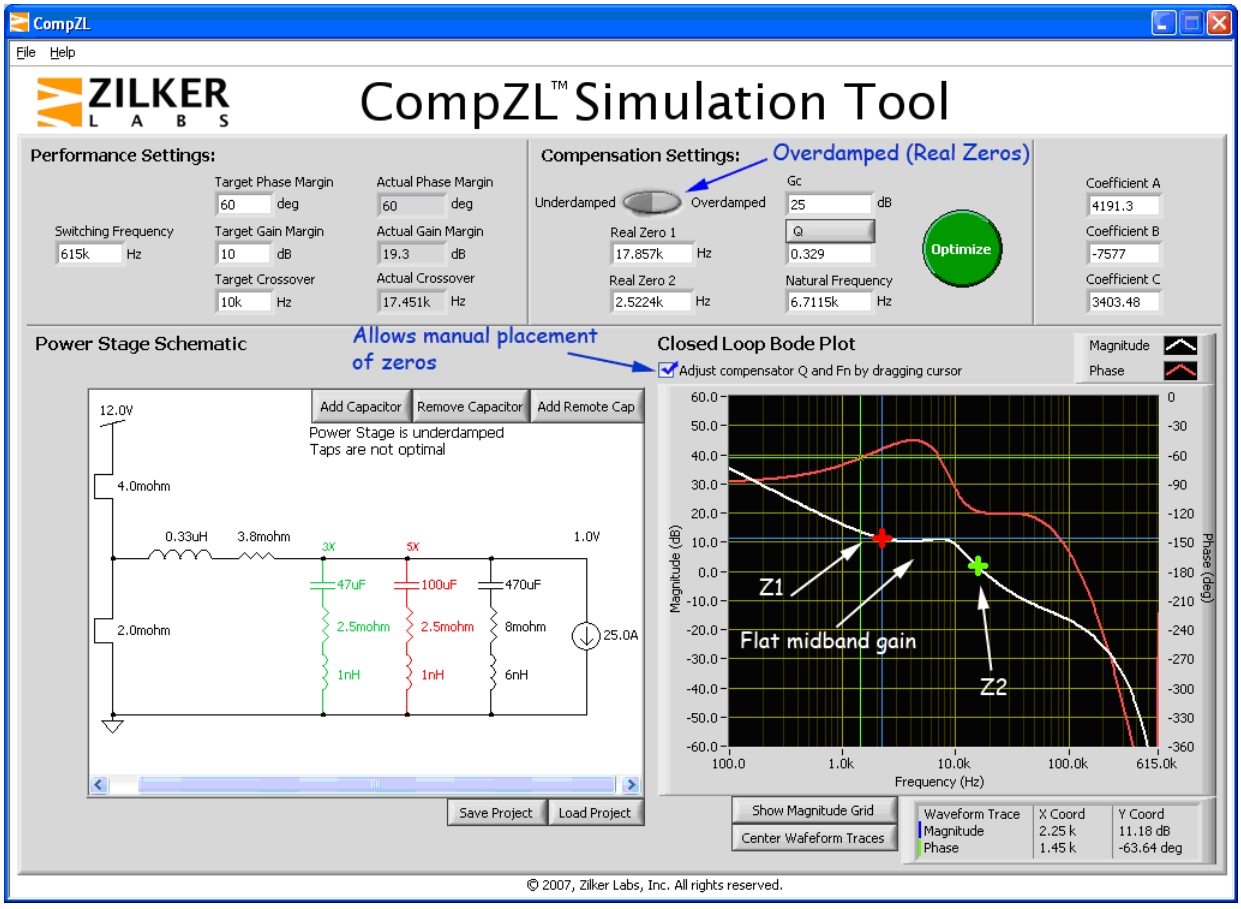

FIGURE 29. USING COMPZL IN THE MANUAL MODE

Configuration Files

Once the hardware design is completed and verified, a configuration file is created for each sharing group controller. The configuration file is composed by using a text editor such as Microsoft Notepad. Other editors can be used as long as the filename has a .txt extension. The configuration file data can utilize both decimal and hexadecimal data. Hexadecimal data is always preceded by 0x. Comments can be added to the configuration file if preceded with a # sign.

Consider the 3-phase sharing group shown in Figure 30. The operating requirements are shown in Table 15.

Configuration files were composed for each phase and are shown in Figure 31. Reference AN2031 “Writing Configuration Files for Zilker” for additional information on composing configuration files.

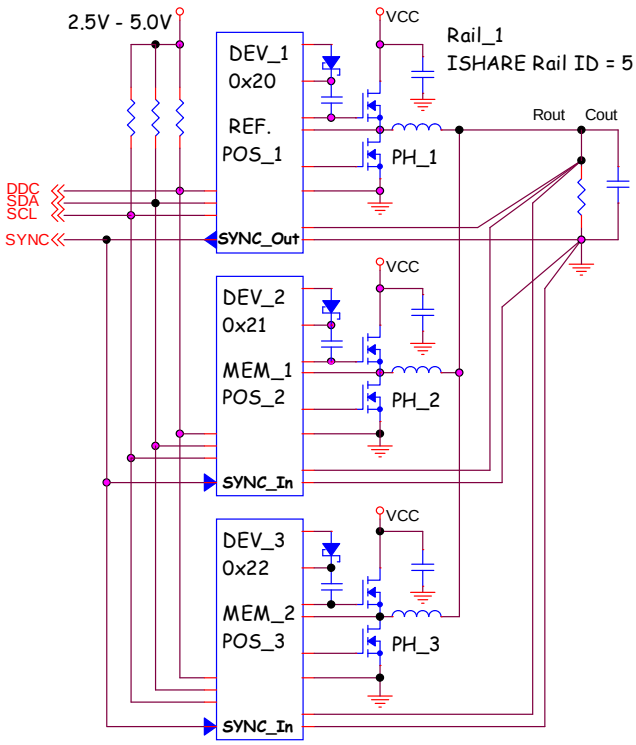

FIGURE 30. 3-PHASE SHARING GROUP EXAMPLE

TABLE 15. 3-PHASE SHARING GROUP REQUIREMENTS

DEVICE (PHASE)	ADDRESS (HEX)	Rail DDC ID	ISHARE Rail ID	SYNC	VIN (V)	V_{OUT} (A)	I_{OUT} (A)	F_{SW} (kHz)
PH_1Ref	0x20	0	5	Source	12	1.0V	25	615
PH_2Mem_1	0x21	1	5	Input	12	1.0V	25	615
PH_2Mem_2	0x22	2	5	Input	12	1.0V	25	615

Configuration File Checklist

Use the following checklist as a guideline when creating configuration files for current sharing rails.

1. Follow memory restore guidelines
   - RESTORE_FACTORY
   - STORE_USER_ALL
   - STORE_DEFAULT_ALL
   - RESTORE_DEFAULT_ALL
   - STORE_DEFAULT_ALL
   - RESTORE_DEFAULT_ALL
2. Assign the same VOUT_DROOP value to all ZL devices in the current sharing group with a value typically between 0.15Ω and 1.0Ω.
3. Ensure that the Time On Delay and Time Off Delay parameters for the reference phase are at least 10ms greater than the delay parameters of each member device.
4. Ensure that each controller in the sharing group has equally configured Time On/Off, Rise/Fall times. Assign the same fault responses for each device.
5. Designate and configure the SYNC source for the group, if the source is one of the group devices all other device(s) in the group are configured as SYNC inputs.
6. Assign the same ISHARE Rail ID to each device in the group using ISHARE_CONFIG.
7. Configure the High to Low and Low to High deadtimes to Freeze using the DEADTIME_CONFIG command.
8. Ensure that each phase of the sharing group has been calibrated for measuring current by using the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands
9. Each sharing group controller has the same configured switching frequency
10. Each sharing group controller has the same current limit configuration.
11. Each sharing group controller has the same fault response configuration.Assign a unique phase position to each group device using ISHARE_CONFIG.
12. Configure Standby Mode to Monitor Enabled for each group member.
13. Set the TEMPCO_CONFIG value for each group member to the same value.
14. Assign the maximum duty cycle to each group device per Equation 6.
15. Configure the Min Duty Cycle command to Enabled.
16. Configure SYNC Time-out EN to SYNC always On.
17. Diode Emulation, Adaptive Frequency Compensation is not supported with current sharing and must be disabled.

Line Number	Command	Reference (Phase_1) Value	Advanced GUI Options
1	RESTORE_FACTORY		
2	STORE_USER_ALL		
3	STORE_DEFAULT_ALL		
4	MFR_ID	Intersil	
5	MFR_MODEL	ZL8101	
6	MFR_REVISION	Ph1_REV_A	
7	MFR_LOCATION	Austin	
8	MFR_DATE		
9	MFR_SERIAL		
10	VOUT_COMMAND	1.0	
11	VOUT_CAL_OFFSET	0.025	
12	VOUT_MAX	1.2	
13	VOUT_MARGIN_HIGH	1.05	
14	VOUT_MARGIN_LOW	0.95	
15	VOUT_DROOP	0.2	
16	IOUT_SCALE	1.083	
17	IOUT_CAL_OFFSET	-1	
18	TON_DELAY	15	
19	TON_RISE	5	
20	TOFF_DELAY	15	
21	TOFF_FALL	5	
22	FREQUENCY_SWITCH	615	
23	VOUT_OV_FAULT_LIMIT	1.4	
24	VOUT_OV_FAULT_RESPONSE	0x80	
25	VOUT_UV_FAULT_LIMIT	0.6	
26	VOUT_UV_FAULT_RESPONSE	0x80	
27	OVUV_CONFIG	0x80	
28	IOUT_OC_FAULT_LIMIT	37	
29	IOUT_AVG_OC_FAULT_LIMIT	25	
30	IOUT_UC_FAULT_LIMIT	-37	
31	IOUT_AVG_UC_FAULT_LIMIT	-25	
32	MFR_IOUT_OC_FAULT_RESPONSE	0x80	
33	MFR_IOUT_UC_FAULT_RESPONSE	0x80	
34	MFR_VMON_OV_FAULT_LIMIT	7	
35	VMON_OV_FAULT_RESPONSE	0x80	
36	MFR_VMON_UV_FAULT_LIMIT	4	
37	VMON_UV_FAULT_RESPONSE	0x80	
38	VIN_OV_WARN_LIMIT	14.3	
39	VIN_OV_FAULT_LIMIT	14.5	
40	VIN_OV_FAULT_RESPONSE	0x80	
41	VIN_UV_WARN_LIMIT	4.4	
42	VIN_UV_FAULT_LIMIT	4	
43	VIN_UV_FAULT_RESPONSE	0x80	
44	OT_WARN_LIMIT	110	
45	OT_FAULT_LIMIT	120	
46	OT_FAULT_RESPONSE	0x80	
47	UT_WARN_LIMIT	-20	
48	UT_FAULT_LIMIT	-30	
49	UT_FAULT_RESPONSE	0x80	
50	AUTO_COMP_CONFIG	0x79	
51	POWER_GOOD_ON	0.8	
52	POWER_GOOD_DELAY	5	
53	DEADTIME_CONFIG	0x8E8E	
54	MAX_DUTY	94	
55	MFR_CONFIG	0x8211	
56	NLR_CONFIG	0x00000000	
57	USER_CONFIG	0x4031	
58	TEMPCO_CONFIG	0x28	
59	MISC_CONFIG	0xE800	
60	INTERLEAVE	0x0000	
61	SEQUENCE	0x0000	
62	DDC_GROUP	0x00000000	
63	DDC_CONFIG	0x010A	
64	ISHARE_CONFIG	0x0541	
66	INDUCTOR	0.2	
67	ON_OFF_CONFIG	0x16	
68	STORE_DEFAULT_ALL		
69	RESTORE_DEFAULT_ALL		

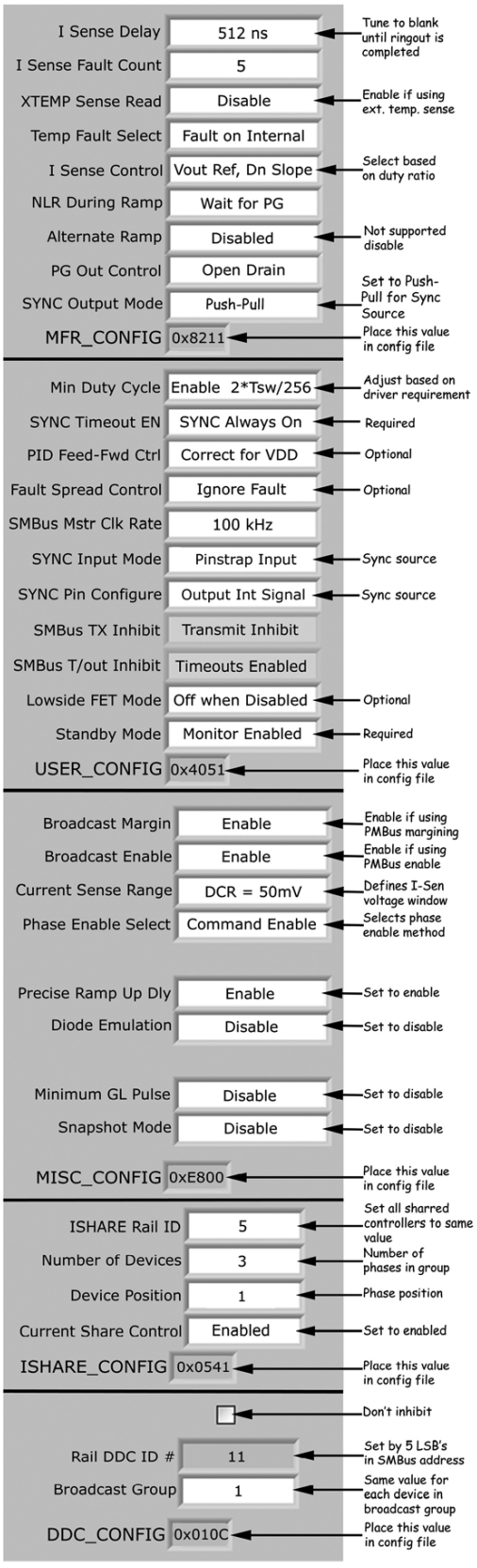

FIGURE 31. CONFIGURATION FILE FOR 3-PHASE CURRENT SHARING GROUP (REF_PHASE)

Member (Phase_2)

Line Number	Command	Value
1	RESTORE_FACTORY	
2	STORE_USER_ALL	
3	STORE_DEFAULT_ALL	
4	MFR_ID	Intersil
5	MFR_MODEL	ZL8101
6	MFR_REVISION	Ph2_REV_A
7	MFR_LOCATION	Austin
8	MFR_DATE	
9	MFR_SERIAL	
10	VOUT_COMMAND	1.0
11	VOUT_CAL_OFFSET	0.025
12	VOUT_MAX	1.2
13	VOUT_MARGIN_HIGH	1.05
14	VOUT_MARGIN_LOW	0.95
15	VOUT_DROOP	0.2
16	IOUT_SCALE	1.083
17	IOUT_CAL_OFFSET	-1
18	TON_DELAY	5
19	TON_RISE	5
20	TOFF_DELAY	5
21	TOFF_FALL	5
22	FREQUENCY_SWITCH	615
23	VOUT_OV_FAULT_LIMIT	1.4
24	VOUT_OV_FAULT_RESPONSE	0x80
25	VOUT_UV_FAULT_LIMIT	0.6
26	VOUT_UV_FAULT_RESPONSE	0x80
27	OVUV_CONFIG	0x80
28	IOUT_OC_FAULT_LIMIT	37
29	IOUT_AVG_OC_FAULT_LIMIT	25
30	IOUT_UC_FAULT_LIMIT	-37
31	IOUT_AVG_UC_FAULT_LIMIT	-25
32	MFR_IOUT_OC_FAULT_RESPONSE	0x80
33	MFR_IOUT_UC_FAULT_RESPONSE	0x80
34	MFR_VMON_OV_FAULT_LIMIT	7
35	VMON_OV_FAULT_RESPONSE	0x80
36	MFR_VMON_UV_FAULT_LIMIT	4
37	VMON_UV_FAULT_RESPONSE	0x80
38	VIN_OV_WARN_LIMIT	14.3
39	VIN_OV_FAULT_LIMIT	14.5
40	VIN_OV_FAULT_RESPONSE	0x80
41	VIN_UV_WARN_LIMIT	4.4
42	VIN_UV_FAULT_LIMIT	4
43	VIN_UV_FAULT_RESPONSE	0x80
44	OT_WARN_LIMIT	110
45	OT_FAULT_LIMIT	120
46	OT_FAULT_RESPONSE	0x80
47	UT_WARN_LIMIT	-20
48	UT_FAULT_LIMIT	-30
49	UT_FAULT_RESPONSE	0x80
50	AUTO_COMP_CONFIG	0x79
51	POWER_GOOD_ON	0.8
52	POWER_GOOD_DELAY	5
53	DEADTIME_CONFIG	0x8E8E
54	MAX_DUTY	94
55	MFR_CONFIG	0x8210
56	NLR_CONFIG	0x00000000
57	USER_CONFIG	0x4051
58	TEMPCO_CONFIG	0x28
59	MISC_CONFIG	0xE800
60	INTERLEAVE	0x0000
61	SEQUENCE	0x0000
62	DDC_GROUP	0x00000000
63	DDC_CONFIG	0x010B
64	ISHARE_CONFIG	0x0545
66	INDUCTOR	0.2
67	ON_OFF_CONFIG	0x16
68	STORE_DEFAULT_ALL	
69	RESTORE_DEFAULT_ALL	

Advanced GUI Options

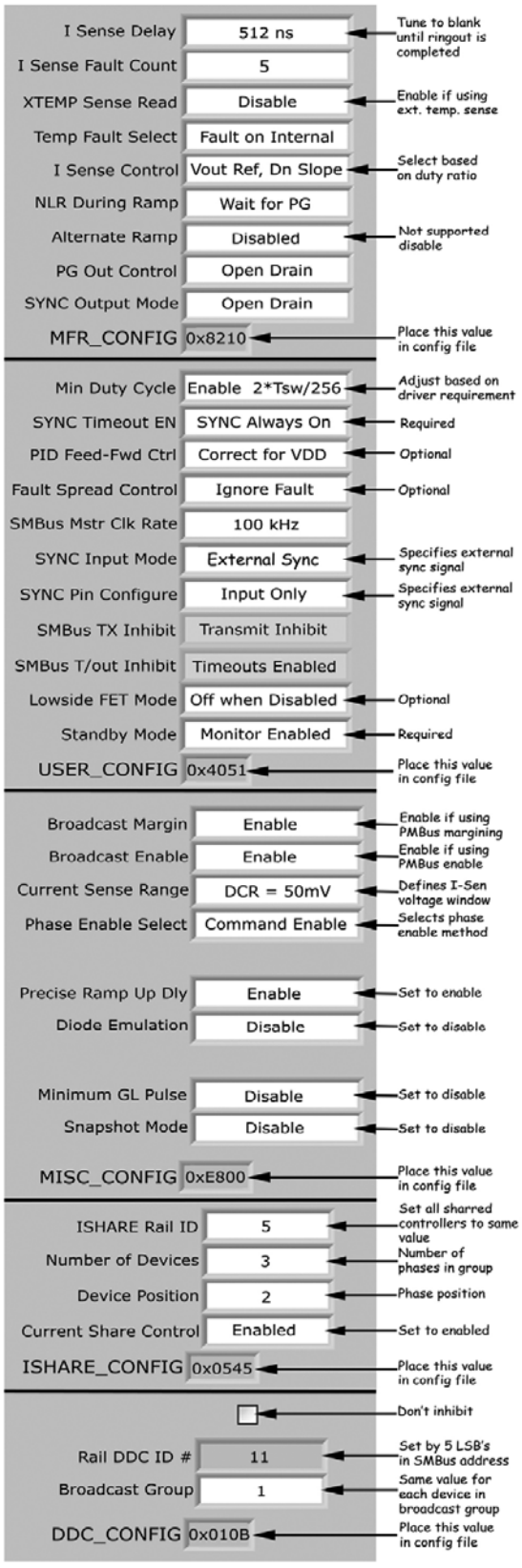

FIGURE 32. CONFIGURATION FILE FOR 3-PHASE CURRENT SHARING GROUP (MEM_1)

Member (Phase_3)

Line Number	Command	Value
1	RESTORE_FACTORY	
2	STORE_USER_ALL	
3	STORE_DEFAULT_ALL	
4	MFR_ID	Intersil
5	MFR_MODEL	ZL8101
6	MFR_REVISION	Ph2_REV_A
7	MFR_LOCATION	Austin
8	MFR_DATE	
9	MFR_SERIAL	
10	VOUT_COMMAND	1.0
11	VOUT_CAL_OFFSET	0.025
12	VOUT_MAX	1.2
13	VOUT_MARGIN_HIGH	1.05
14	VOUT_MARGIN_LOW	0.95
15	VOUT_DROOP	0.2
16	IOUT_SCALE	1.083
17	IOUT_CAL_OFFSET	-1
18	TON_DELAY	5
19	TON_RISE	5
20	TOFF_DELAY	5
21	TOFF_FALL	5
22	FREQUENCY_SWITCH	615
23	VOUT_OV_FAULT_LIMIT	1.4
24	VOUT_OV_FAULT_RESPONSE	0x80
25	VOUT_UV_FAULT_LIMIT	0.6
26	VOUT_UV_FAULT_RESPONSE	0x80
27	OVUV_CONFIG	0x80
28	IOUT_OC_FAULT_LIMIT	37
29	IOUT_AVG_OC_FAULT_LIMIT	25
30	IOUT_UC_FAULT_LIMIT	-37
31	IOUT_AVG_UC_FAULT_LIMIT	-25
32	MFR_IOUT_OC_FAULT_RESPONSE	0x80
33	MFR_IOUT_UC_FAULT_RESPONSE	0x80
34	MFR_VMON_OV_FAULT_LIMIT	7
35	VMON_OV_FAULT_RESPONSE	0x80
36	MFR_VMON_UV_FAULT_LIMIT	4
37	VMON_UV_FAULT_RESPONSE	0x80
38	VIN_OV_WARN_LIMIT	14.3
39	VIN_OV_FAULT_LIMIT	14.5
40	VIN_OV_FAULT_RESPONSE	0x80
41	VIN_UV_WARN_LIMIT	4.4
42	VIN_UV_FAULT_LIMIT	4
43	VIN_UV_FAULT_RESPONSE	0x80
44	OT_WARN_LIMIT	110
45	OT_FAULT_LIMIT	120
46	OT_FAULT_RESPONSE	0x80
47	UT_WARN_LIMIT	-20
48	UT_FAULT_LIMIT	-30
49	UT_FAULT_RESPONSE	0x80
50	AUTO_COMP_CONFIG	0x79
51	POWER_GOOD_ON	0.8
52	POWER_GOOD_DELAY	5
53	DEADTIME_CONFIG	0x8E8E
54	MAX_DUTY	94
55	MFR_CONFIG	0x8210
56	NLR_CONFIG	0x00000000
57	USER_CONFIG	0x4051
58	TEMPCO_CONFIG	0x28
59	MISC_CONFIG	0xE800
60	INTERLEAVE	0x0000
61	SEQUENCE	0x0000
62	DDC_GROUP	0x00000000
63	DDC_CONFIG	0x010C
64	ISHARE_CONFIG	0x0549
66	INDUCTOR	0.2
67	ON_OFF_CONFIG	0x16
68	STORE_DEFAULT_ALL	
69	RESTORE_DEFAULT_ALL	

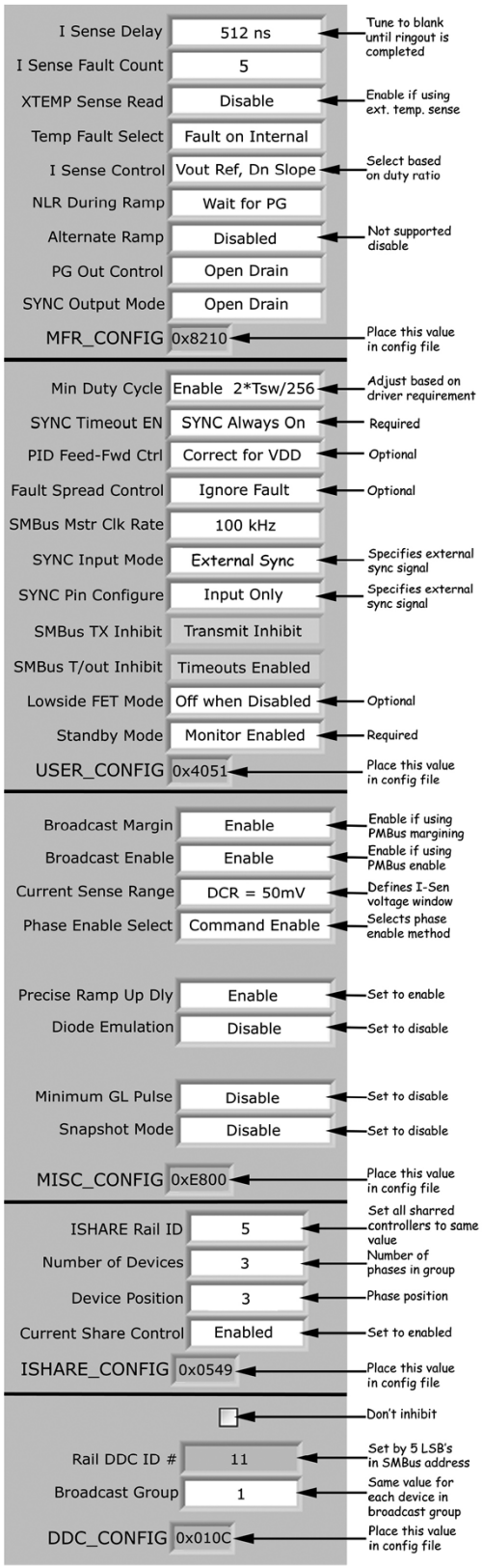

FIGURE 33. CONFIGURATION FILE FOR 3-PHASE CURRENT SHARING GROUP (MEM_2)

Appendix

TABLE 16. DDC RAIL ID# vs SMBus ADDRESS

PMBus Address	Binary	5 LSB's	Rail DDC ID
0x20	00100000	00000	0
0x21	00100001	00001	1
0x22	00100010	00010	2
0x23	00100011	00011	3
0x24	00100100	00100	4
0x25	00100101	00101	5
0x26	00100110	00110	6
0x27	00100111	00111	7
0x28	00101000	01000	8
0x29	00101001	01001	9
0x2A	00101010	01010	10
0x2B	00101011	01011	11
0x2C	00101100	01100	12
0x2D	00101101	01101	13
0x2E	00101110	01110	14
0x2F	00101111	01111	15
0x30	00110000	10000	16
0x31	00110001	10001	17
0x32	00110010	10010	18
0x33	00110011	10011	19
0x34	00110100	10100	20
0x35	00110101	10101	21
0x36	00110110	10110	22
0x37	00110111	10111	23
0x38	00111000	11000	24
0x39	00111001	11001	25
0x3A	00111010	11010	26
0x3B	00111011	11011	27
0x3C	00111100	11100	28
0x3D	00111101	11101	29
0x3E	00111110	11110	30
0x3F	00111111	11111	31

TABLE 17. ISHARE_CONFIG

BITS	PURPOSE	VALUE	DESCRIPTION
15:8	IShare Rail ID	0	Sets the current share rail's DDC ID for each device within a current share rail. Set to the same DDC ID as in DDC_CONFIG. This DDC ID is used for sequencing and fault spreading when used in a current share rail.
7:5	Number of Devices	1	Number of devices in current share rail -1
4:2	Device Position	1	Position of device within current share rail
1	Reserved	0	Reserved.
0	Current Share Control	0	0 = Device is not a member of a current share rail
			1 = Device is a member of a current share rail